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INVENTOR(S)

Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
MICHAEL S.	Mc CORQUODALE	ANN ARBOR, MICHIGAN

Additional inventors are being named on the _____ separately numbered sheets attached hereto

TITLE OF THE INVENTION (500 characters max)

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ENCLOSED APPLICATION PARTS (check all that apply)

[X] Specification Number of Pages 335   [ ] CD(s), Number _____

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[ ] Application Data Sheet. See 37 CFR 1.76

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[Page 1 of 2]

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1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
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1253	950	2253	475	Extension for reply within third month	
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1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
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1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
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| Name (Print/Type) | NANCY R. GAMBURD | Registration No. (Attorney/Agent) | 38,147 | Telephone | 312-551-4925 |

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MONOLITHIC AND TOP-DOWN CLOCK SYNTHESIS
WITH MICROMACHINED RADIO FREQUENCY REFERENCE

by

Michael Shannon McCorquodale

A dissertation submitted in partial fullfillment
of the requirements for the degree of
Doctor of Philosophy
(Electrical Engineering)
in the University of Michigan
2004

Doctoral Committee:

Richard B. Brown, Professor, Chair
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For all who have fervently supported me in every endeavor that I have undertaken.

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In my years at Michigan I have had the pleasure of working with many talented and inspiring individuals from a variety of disciplines. Each and every one of these individuals has impacted my research and the quality of my experience here in a very positive manner and for that, I am eternally grateful. However, of these people, I believe that I owe the deepest gratitude to my faculty advisor, Dr. Richard Brown. His unwavering support for even my most grandiose endeavors has allowed me to discover my personal strengths as well as my proclivity toward overcommittment and all of the corresponding frustrations that result. Yet without Dr. Brown's guidance, I am certain that my experience at Michigan would not have been as colorful and broad as it was, and the breadth of these experiences is truly the highlight of my time here.

Within Dr. Brown's research group I have had the pleasure of pursuing collaborative research with several very talented engineers including Keith Kraver, Fadi Gebara, Eric Marsman, and Rob Senger. The research that stemmed from these collaborative activities demonstrated, without a doubt, that much more meaningful academic contributions can be achieved by those who work toward a common goal than by those who work independently. Moreover, I believe that the interdisciplinary knowledge and perspective acquired through these interactions greatly enhanced each of our individual research pursuits.

In addition to these individuals, I am particularly grateful to Mei Kim (Joanne) Ding who was by far the best undergraduate research assistant with whom I have ever worked. Joanne's initiative, work ethic, and diligence lead to great strides in my research. Moreover, her efforts gave rise to the "Joanne factor," a metric against which all other undergraduate student researchers are apparently now measured.

Along those lines, I am also very grateful to Jim McCann who was also an outstanding undergraduate research assistant. His work led to the development of the GUI for *Newton*, which is presented within this dissertation. With quite minimal input, Jim took a nebulous concept and literally turned it into a work of art.

ABSTRACT

MONOLITHIC AND TOP-DOWN CLOCK SYNTHESIS WITH MICROMACHINED

RADIO FREQUENCY REFERENCE

By

Michael Shannon McCorquodale

Chair: Richard B. Brown

This dissertation explores the techniques by which clock synthesis for embedded processors can be achieved in monolithic form while maintaining high frequency accuracy and stability. Motivation for this work includes the potential for substantial reductions in overall microelectronic system power dissipation, size, and cost through complete integration of the clock synthesis function.

A thorough treatment of phase noise and jitter, particularly as these topics apply to clock synthesis, is presented in this work. The effects of frequency translation on stability are also analyzed and a new systemic top-down clock synthesis approach is presented as a consequence of this analysis. Harmonic oscillators are identified as the best solution for stable and accurate top-down clock synthesis. Consequently, micromachining techniques for RF passive devices are explored in an effort to develop a precision harmonic reference for this work. A maskless post-process for fabricating RF MEMS components in commercial CMOS is presented successfully. Both micromechanical varactors and suspended inductors are shown. The tuning range of the developed micromechanical varactors is shown to be up to 18%. Additionally, the inductor quality factor is shown to improve by up to 13% using the techniques shown here.

A successful prototype of a complete monolithic harmonic clock synthesizer is demonstrated with these passive devices. The synthesizer generates frequencies from

28MHz to 900MHz in increments of 2. The maximum RMS jitter for all frequencies is shown to be less than 300ppm while the power dissipation is less than 15mW. Tuning of up to 2.2% is also demonstrated using a novel frequency-pulling approach to frequency trimming.

The remainder of this dissertation focuses on implementation of the developed clock synthesizer into an embedded system. Advances in the area of design automation and IP-based design have been developed throughout this effort. A top-down microsystems methodology has been proposed and a software tool has been developed for the synthesis of MEMS devices related to this research and in support of the developed methodology. The clock synthesizer is demonstrated successfully as the sole clock reference for an embedded processor where the clock frequencies can be switched nearly instantaneously between any two frequencies in the range of 2kHz to 66MHz. All of these frequencies are synthesized from a 1.1GHz reference.

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CHAPTER I

INTRODUCTION

At the 2003 International Solid-State Circuits Conference Chris Mangelsdorf, of *Analog Devices*, confidently exclaimed, "integration always wins!" He went on to claim that if a company set out to implement a multi-chip module, the competitor that pursued a single-chip solution would succeed and win the market [1]. With these simple words, Mangelsdorf has captured the essence of this dissertation. Nearly every single electronic system today includes some combination of mechanical, analog, and digital technologies—with some now including optical, biological, and chemical technologies as well. These systems are currently assembled with multiple components on a printed circuit board, rather than integrated onto a common substrate and as a single circuit. Consequently these systems are large, expensive, high-power, complicated, unreliable, and functionally limited as compared to an integrated implementation. Indeed Mangelsdorf was correct in his observation as improvement over these metrics through integration has driven the trend for the past thirty-five years in the microprocessor market, shown in Figure 1.1. The latest challenges involve not just the integration of transistors, but the integration of technologies from disparate domains such as the mechanical and biological domains. The field of microsystems has emerged to address these challenges. The European Union defines microsystems as systems comprising sensing, processing and/or actuating functions where two or more of the following technologies are combined onto a single chip: electrical, magnetic, mechanical, optical, chemical, or biological [2]. Microsystems exploit the benefits of integration including reduced power, size, and complexity, while providing greater functionality at significantly less cost.

Upon examination of a generalized electronic system, like that pictured in Figure 1.2, one can observe several subsystems that are currently discrete. Many exciting

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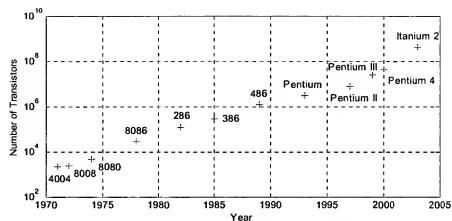
Figure 1.1 Transistor count per die for *Intel* processor products over the past 35 years. The trend is exponential and is commonly called Moore's Law, after Gordon Moore of *Intel*, who first identified the trend.

fields of research have spawned from this observation. For example, radio frequency (RF) complementary metal-oxide-semiconductor (CMOS) technology is a field that has recently exploded in an effort to merge RF communication circuits with the baseband processor. Even emerging specifications, such as *Bluetooth*, have been developed specifically to facilitate this convergence of CMOS RF electronics with the processor. CMOS analog and RF circuit design is also a topic which now receives a significant amount of attention, and is the entire topic of recent text books such as [3] and [4].
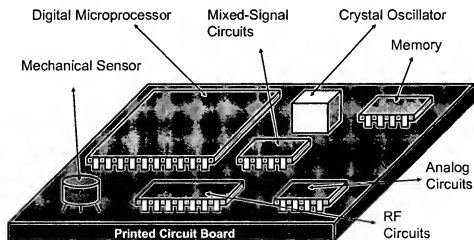
Figure 1.2 A generalized modern electronic system assembled on a printed circuit board from several disparate components.

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Despite the efforts in these fascinating research fields, which have led to great strides in the realization of monolithic systems, one significant component continues to be overlooked. This component is the clock reference and the supporting electronics for clock generation which drive the processor and other circuits in the system. The integration of the clock synthesizer, using microsystems technology, is the focus of this dissertation.

1.1 Clock Synthesis

Virtually all modern microelectronic processors and microcontrollers are synchronous. The term synchronous refers to the relationship between two or more repetitive signals that have simultaneous occurrences of significant instants [5]. Specifically, these significant instants are the system clock transitions. In any processor, at one or both transitions, the clock signal captures and stores data in several sequential logic circuits at once. This approach comprises the fundamental basis of synchronous processing.

The ability to capture and store data is wholly contingent upon the system clock. The clock is the reference source of timing information. One can argue that the clock is the most significant signal in a synchronous system. It paces a number of important activities including the sampling rate in data conversion circuits and framing and timing information in communication circuitry. In a microprocessor application, the clock is a device that generates periodic, accurately-spaced signals used for such purposes as timing, regulation of the operations of a processor, or generation of interrupts [5].

1.2 Motivation for Integration

The benefits associated with high levels of microelectronic integration are many. First and foremost is cost reduction. It has been estimated that a considerable portion of the cost associated with an integrated circuit (IC) is for the packaging of that circuit [6]. Therefore, in any system, if the number of components can be reduced, the overall system cost can also be reduced dramatically. Also of significant importance is power dissipation, especially considering the current ubiquity of portable devices. The power required to transmit signals across a printed circuit board is approximately an order of magnitude larger than the power required to transmit signals internally on an IC. Significant power savings can therefore be obtained through integration at the IC level. Lastly, in many applications, size and weight

are paramount and integration can significantly reduce both the size and weight of micro-electronic systems, by replacing macroscopic devices with microscopic equivalent circuits.

Significant research and development efforts toward microelectronic integration have been underway for many years. However, most microelectronic systems still contain several macroscopic mechanical components as well as transistor circuits fabricated on substrates that are incompatible with Si, such as SiGe and InP. Moreover, as systems become increasingly integrated, digital, analog, and mixed-signal functions must be incor-porated onto the same chip and there are many challenges associated with merging these technologies onto a common substrate.

Microelectromechanical systems (MEMS) technology has recently come to the forefront of microelectronic and semiconductor research. MEMS hold the potential to inte-grate macroscopic mechanical components with transistor electronics. This is achieved by building these components at the micro-scale while making them compatible with transis-tor fabrication process technology. Thus, a complete system-on-chip (SoC) or microsystem can be realized. Much MEMS research to date has been in the area of sensors and actuators as well as optical MEMS. However, many other applications of miniaturized electrome-chanical devices are emerging, such as those that will be discussed within this dissertation.

1.3 A Research Application

The clock generation research that is presented in this work is part of a much larger research application and context. The clock synthesizer developed here has been deployed as the sole clock reference for a complete 16-bit mixed-signal microsystem. The microsystem has been developed to support two general testbeds, environmental and biological, which are the focus of the work in the Wireless Integrated Microsystems (WIMS) Engineering Research Center (ERC) at the University of Michigan. Environmental applications include heavy metal ion sensing for pollution control and gas chromatography. An artist's rendition of such a system is illustrated in Figure 1.3. In the biological area, applications include deep brain implants for neural stimulus and cochlear implants for the hearing impaired.

The clock generation research pursued here ultimately allows the processor that has been developed for these applications to operate without external components and with

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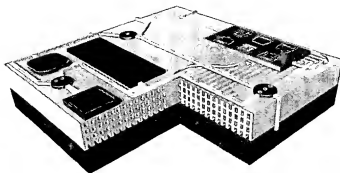
Figure 1.3   Illustration of the environmental gas chromatography as an integrated microsystem [7].

reduced power dissipation. Eliminating external components and reducing power ultimately reduces the size of the processor for these applications, which is clearly paramount. Many other research activities within the Center are also focused at integrating key functions for these applications.

1.4 Thesis Overview

The focus of this dissertation is the development of a monolithic technology for clock synthesis. Chapter II begins with a review of critical metrics for clock synthesis systems. Oscillator theory, classes, and topologies are then presented along with state-of-the-art techniques for clock synthesis. Chapter III presents a systemic analysis of clock synthesis with a focus on frequency stability including a new and top-down frequency synthesis approach. Chapter IV, presents current research activities in the field of monolithic oscillators, with a focus on micromachined technologies. Chapter V presents a complete description of the developed monolithic clock synthesis system. The development of a CMOS-compatible electrically resonant harmonic micromechanical reference is described. The fabrication technology for this reference is also presented. The reference has been deployed into a monolithic CMOS circuit using several advanced circuit design techniques in an effort to mitigate noise. Data collected from fabricated devices is presented along with simulation and theoretical data. All results are summarized and compared. Chapter VI focuses on the development of the clock synthesis system into a large-scale mixed-signal microcontroller design. A thorough discussion of design methodologies is presented and the need for mixed-signal and MEMS synthesis is presented. An intellectual property (IP)-

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based design approach has been used in the development of this microcontroller and the development of IP blocks including MEMS and mixed-signal technologies is presented. Chapter VII describes *Newton*, a synthesis tool for the development of the micromachined devices presented in this work and several other micromechanical technologies. Algorithms developed for this tool are presented along with verified results from synthesis, fabrication, and test. This dissertation closes with suggested future work based on the results presented.

CHAPTER II

CLOCK SYNTHESIS THEORY AND TECHNOLOGY

Several different clock synthesis technologies exist in modern microelectronic systems, yet all are based on a reference signal. This signal is typically translated, through frequency division or multiplication, by additional circuitry in order to synthesize the desired signals for the application. The reference signal is often developed from a reference device or group of devices that possess distinct frequency-selective properties typically based on some form of mechanical or electrical resonance. However, in some cases the reference is based on an inherent property of the reference circuit. For example, the fundamental frequency of a ring oscillator is set by the total delay around the ring. In contrast, quartz crystals and lithium niobate ($LiNbO_3$) surface acoustic wave (SAW) devices both operate on the principle of mechanical resonance through piezoelectric effect. When an electric field is applied across these devices, the material deforms at a distinct frequency. This deformation induces a current that can be amplified and sustained with feedback by active electronics and then used as the reference signal. The device, along with this sustaining amplifier, is called the reference oscillator. The reference oscillator signal can then be frequency translated by additional electronics such as a phase-locked loop (PLL) or delay-locked loop (DLL). These components—the reference, the sustaining amplifier, and the frequency translation circuitry—comprise the elements necessary for clock synthesis. A functional schematic of such an implementation is shown in Figure 2.1.

The ubiquitous reference device for clock generation is the quartz crystal. A reference oscillator, based on this device, coupled with a PLL or DLL is the most common clock synthesis topology in modern microelectronic systems. However, quartz is a material that cannot be fabricated along with the integrated devices that comprise the sustaining amplifier and the frequency translation circuitry. Additionally, quartz crystals are macroscopic

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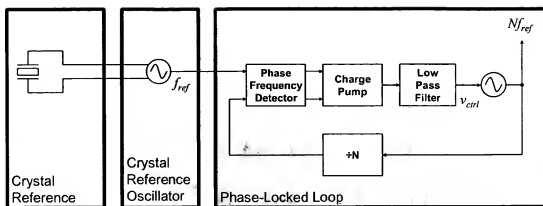
Figure 2.1 Functional schematic of a clock synthesis system including the crystal reference, reference oscillator, and the PLL.

devices. Quartz also does not scale well with frequency because these devices operate in bulk vibrational modes via bulk acoustic waves (BAW) and thus the thickness of the device must decrease in order to increase the resonant frequency. However, thin quartz devices are difficult to manufacture and can fracture easily if overdriven by an electrical signal [3]. $LiNbO_3$ SAW devices, in contrast, operate through excitation from surface acoustic waves and thus the effective thickness is much smaller than the physical thickness. These devices have been used successfully at high frequencies where quartz is not an option. Yet $LiNbO_3$ also cannot be fabricated with the accompanying integrated devices. Consequently, several emerging technologies have been developed recently in an effort to completely eliminate reference devices like quartz and $LiNbO_3$ and thus achieve monolithic integration. These reference technologies include MEMS resonant cavities [8], mechanical MEMS resonators [9], and MEMS piezoelectric materials [10], all of which are described in subsequent chapters. Additionally, several simple monolithic circuit approaches have existed for years including the ring oscillator.

This chapter begins with a brief review of noise processes in CMOS electronics. This basic review will facilitate understanding of the subsequent sections where thorough descriptions of the critical metrics pertaining to clock synthesis are presented. The chapter continues with a review of oscillator theory along with common oscillator topologies. The chapter closes with a qualitative survey of state-of-the-art technology for clock synthesis in microelectronic systems.

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2.1 Noise in CMOS Microelectronics

Several different noise processes exist in microelectronics including shot, burst, avalanche, thermal, and flicker noise. Shot and avalanche noise do not exist in CMOS devices and burst noise will not be considered. Thermal and flicker noise are most pertinent to this work and it will be shown subsequently how these processes affect the stability of oscillators. For now, it is important to simply understand the characteristic behavior of each noise process. In the two sections that follow, the most significant observations include the origins of each noise process and the respective spectrum for each noise process. It will be shown later that even low-frequency noise sources can greatly affect the performance of high-frequency oscillators.

2.1.1 Thermal Noise

Thermal noise is associated with the random thermal movement of charge carriers through any resistive medium. The noise process is also independent of current. As would be expected, the process is related to temperature and is, in fact, directly proportional to temperature. The variance of this noise process can be represented by either an equivalent current or voltage source as shown in Figure 2.2 and can be expressed mathematically by,

$$\overline{v^2} = 4kTR\Delta f \tag{2.1}$$

$$\overline{i^2} = \frac{4kT}{R}\Delta f \tag{2.2}$$

where k is Boltzmann's constant, T is temperature, R is the resistance the device, and Δf is the bandwidth. Given (2.1) and (2.2) it is clear that the thermal noise spectrum is white, as shown in Figure 2.2.

2.1.2 Flicker Noise

Flicker noise exists in all active devices. It arises from charge carrier trapping sites. These trapping sites exist due to contamination and defects within the conductive material. In CMOS electronics, flicker noise is almost exclusively due to trapping sites that exist at the

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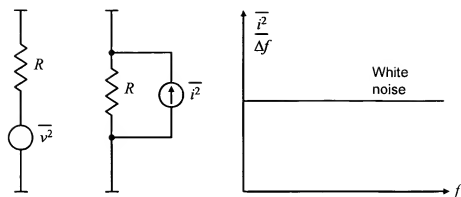
Figure 2.2 Schematic of thermal noise equivalent noise generators based upon the variance of the noise process. Thermal noise is constant over frequency and thus termed white noise.

Si and SiO$_2$ interface within the induced channel of the device. These sites, randomly trap and release charge carriers as they flow across the channel. Thus, flicker noise is only present when a DC current exists. Furthermore, it is a low frequency phenomenon. The variance of a flicker noise process is given by,

$$\overline{i^2} = K\frac{I}{f^\alpha}\Delta f \tag{2.3}$$

where K is an empirical constant, I is the DC current in the device, f is frequency, and α is the exponent of f, typically near 1.

Figure 2.3 shows the power spectral density (PSD) of a flicker noise source. Because the spectrum varies with frequency, it is commonly called colored noise or pink noise. The latter term arises from the fact that visible light shaped by a $1/f$ spectrum is pink.

2.1.3 Comments on Noise

It is difficult to reduce or eliminate the noise that arises from the phenomena just described. For example, thermal noise could be reduced by lowering the operating temperature of the electronics. In fact, in some applications, this technique is actually employed. However, this is typically impractical in applications where size and power are constraints.

Some increased flexibility exists with flicker noise where reducing the DC current reduces the noise, as does somehow reducing the trap density. In fact, the latter approach

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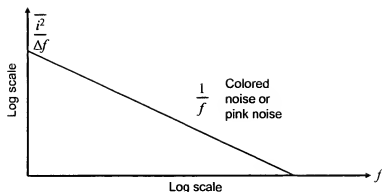
Figure 2.3 Power spectral density of flicker noise. The majority of the noise power exists at low frequencies. Flicker noise is commonly termed colored or pink noise due to the $1/f$ shape.

is explored in the development of the oscillator used in this work. For now, though it is not obvious, it suffices to mention that some techniques can be employed to improve the noise performance of microelectronic circuits.

2.2 Critical Metrics

Every clock generation technology must provide a stable, accurate, and precise periodic signal over a range of environmental conditions. In the discussion that follows, several metrics are presented that quantify this intuitive and qualitative notion.

2.2.1 Short-Term Frequency Stability

The short-term frequency stability of an oscillator characterizes the deviation of the oscillation frequency over a short period of time. Device and environmental noise are the primary contributing factors to short-term frequency instability.

Frequency stability is particularly critical in the area of clock generation because instability cuts directly into the timing budget for any synchronous logic circuit, such as a microprocessor. Consider the critical path of a generic synchronous system, illustrated in Figure 2.4. The maximum clock frequency is set by the minimum clock cycle. Without jitter, the minimum cycle is the sum of the delay through the flip-flop, the delay through the combinatorial logic, the setup time required for the second flip-flop, and the skew. Jitter may cause the first edge to occur late and the second edge to occur early, thus cutting

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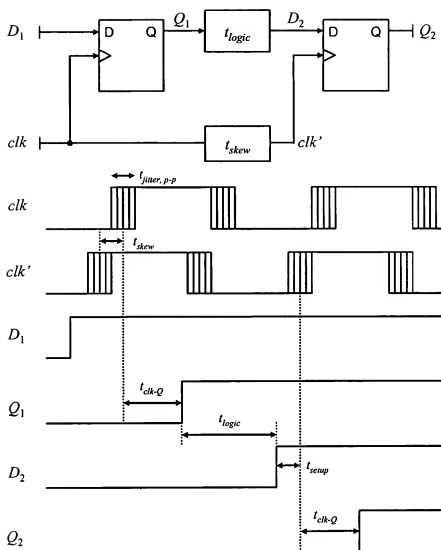
Figure 2.4   Illustration of the critical path in a synchronous system. The maximum clock frequency is set by the minimum clock cycle. Without jitter, the minimum cycle is the sum of the delay through the flip-flop, the delay through the combinatorial logic, the setup time required for the second flip-flop, and the skew. Jitter may cause the first edge to occur late and the second edge to occur early, thus cutting directly into the timing budget.

directly into the timing budget. Thus, for each edge, half of the peak-to-peak jitter, $t_{jitter,\,p-p}$, must be added to the minimum cycle. Using the notation in Figure 2.4, the maximum clock frequency for the system can be calculated by,

$$f_{max} = \frac{1}{t_{cycle,\,min}} = \frac{1}{t_{clk-Q} + t_{logic} + t_{setup} + t_{skew} + t_{jitter,\,p-p}} \qquad (2.4)$$

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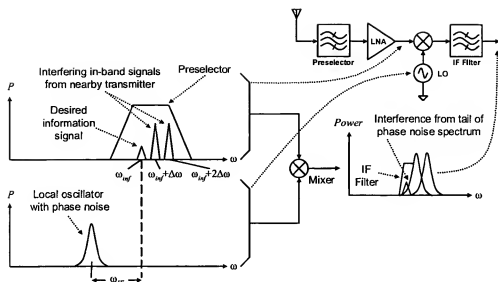
Figure 2.5 A generic superheterodyne RF receiver front-end. Signals are first filtered by a wideband preselector. High-power in-band interfering signals are passed along with the desired signal. The signals are then mixed to the IF by a LO with phase noise. If the LO exhibits high phase noise, the in-band interfering signals will be reciprocally mixed and block the desired signal. In this figure, P is power, ω is radian frequency, ω_{inf} is the frequency at which the desired information exists, $\Delta\omega$ is the channel spacing, and ω_{if} is the intermediate frequency.

Clearly, the frequency instability of the clock directly affects the maximum operational frequency of the system. Thus it is important to characterize clock stability, understand the factors that contribute to instability, and ultimately minimize this instability.

Short-term frequency instability is also of critical importance in RF systems. For example, consider a generic superheterodyne RF receiver as shown in Figure 2.5. Here a preselecting filter passes a band of frequencies from the antenna to the low noise amplifier (LNA). Often the desired signal will be in-band with several nearby high-power interfering signals. All preselected signals are then amplified and mixed with the local oscillator (LO) to the intermediate frequency (IF). The desired channel is selected by the narrowband IF filter. An LO with poor short-term stability, or high phase noise, will mix the in-band interfering signals, thus masking the desired signal. This phenomenon is called reciprocal mixing. Phase noise is another metric that quantifies the short-term stability of oscillators and both phase noise and jitter are described in detail next.

Phase noise defines the noise power spectrum, P, around the fundamental frequency as shown in Figure 2.6. In the ideal case, the spectrum is a Dirac-delta function at the fun-

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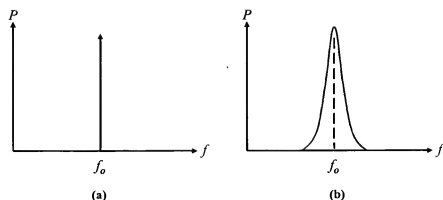
Figure 2.6   Power output spectrum of an oscillator illustrating the concept of phase noise, a frequency-domain metric. (a) Ideal output spectrum of an oscillator. (b) Typical oscillator output spectrum with phase noise where finite power is spread around f_o.

damental output frequency f_o. Practically, due to device noise, the oscillator output spectrum exhibits noise power around the fundamental frequency.

Jitter metrics quantify the time-domain uncertainty in the oscillator period. Ideally, edges of the oscillator signal occur at identical intervals in time as shown by the voltage waveform in Figure 2.7. In practical circuits, the edges of the signal deviate from this ideal position by some amount each cycle.

In the sections that follow, a thorough treatment of phase noise and jitter will be presented, as will relationships that permit conversion from one metric to the other.
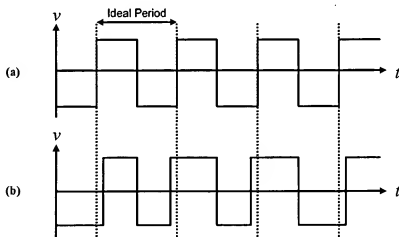
Figure 2.7   Time-domain voltage waveform of an oscillator illustrating the concept of jitter, a time-domain metric. (a) Ideal waveform. (b) Waveform with jitter showing variations in the position of the rising and falling edges of the signal.

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2.2.1.1 Phase Noise

Consider the ideal voltage output, $v_o(t)$, of an autonomous oscillator as a function of time, t. This signal can be expressed as,

$$v_o(t) = V_1 \cos(\omega_o t) \tag{2.5}$$

where ω_o is the fundamental radian frequency and V_1 is the nominal voltage amplitude. The output of the same oscillator, under the influence of noise processes, can then be described by,

$$v_n(t) = [V_1 + \varepsilon(t)] \cos[\omega_o t + \phi(t)] \tag{2.6}$$

where $\varepsilon(t)$ and $\phi(t)$ are, in the most general sense, zero-mean stochastic processes. Typically, fluctuations in the amplitude of the oscillator signal are ignored as they can be removed with the introduction of a limiter. Therefore, $\phi(t)$ is the only process of concern when considering phase noise. The power spectral density (PSD) of $\phi(t)$, $S_\phi(f)$, describes the frequency-domain noise power of this process. However, in practice, the voltage power spectral density, $S_{v_n}(f)$, is measured with a spectrum analyzer. Then the single-sideband phase noise PSD, $(N_o/P_o)_{f_m}$, is described as the noise power relative to the fundamental power, P_o, at the fundamental frequency, f_o, for some offset f_m, and is given by the following expression,

$$\left(\frac{N_o}{P_o}\right)_{f_m} = \frac{S_{v_n}(f_o + f_m)}{P_o} \tag{2.7}$$

The phase noise PSD exhibits specific behavior relative to the frequency offset from the fundamental. Five distinct regions can be described by the exponential relationship to frequency. Considering noise power as a function of frequency away from the fundamental, these regions and the associated proportional relationships are:

- Random walk of frequency $\propto 1/f^4$

- Flicker of frequency $\propto 1/f^3$

- White of frequency or random walk of phase $\propto 1/f^2$

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- Flicker of phase $\propto 1/f^1$

- White of phase $\propto 1/f^0$

In practice, only white of frequency and flicker of frequency phase noise are of primary concern as these two regions span the greatest bandwidth. Additionally, in RF systems, the offset frequencies at which this type of phase noise is observed often corresponds to the frequencies of potential blocking signals. Figure 2.8 illustrates the phase noise spectrum for a typical oscillator exhibiting all five types of phase noise.

It is useful and insightful to relate $(N_o/P_o)_{f_m}$ to $S_\phi(f)$ because although $(N_o/P_o)_{f_m}$ is typically measured, $S_\phi(f)$ is the actual phase noise power spectral density of $\phi(t)$. Consider $v_n(t)$ as in (2.6) again, but without amplitude noise and in the form,

$$v_n(t) = v_o\left(t + \frac{\phi(t)}{2\pi f_o}\right) \qquad (2.8)$$

The expression in (2.8) can be approximated by a Taylor series expansion as follows,

$$v_n(t) \approx v_o(t) + \frac{\mathrm{d}}{\mathrm{d}t}v_o(t)\frac{\phi(t)}{2\pi f_o} \qquad (2.9)$$

Recall that $v_o(t)$ is periodic and thus it can be written as a Fourier series,
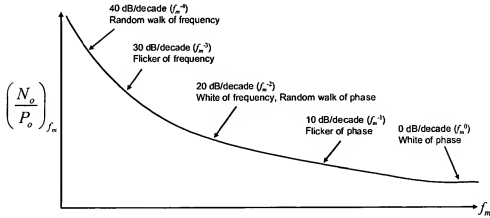
Figure 2.8   Characteristic behavior of phase noise in an autonomous oscillator as a function of frequency offset from the fundamental. The flicker of frequency and white of frequency regions span the majority of the spectrum.

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$$v_o(t) = \sum_{k=-\infty}^{\infty} V_k e^{j2\pi k f_o t} \tag{2.10}$$

Substituting (2.10) into (2.9) yields,

$$v_n(t) \approx \sum_{k=-\infty}^{\infty} V_k e^{j2\pi k f_o t} + \frac{\phi(t)}{2\pi f_o} \sum_{k=-\infty}^{\infty} j2\pi k f_o V_k e^{j2\pi k f_o t} \tag{2.11}$$

which can be reduced to,

$$v_n(t) \approx \sum_{k=-\infty}^{\infty} V_k e^{j2\pi k f_o t} + \phi(t) \sum_{k=-\infty}^{\infty} jk V_k e^{j2\pi k f_o t} \tag{2.12}$$

The expression in (2.12) is of the form $v_n(t) \approx v_o(t) + n(t)$, where $n(t)$ can now be considered as additive noise. The PSD of $n(t)$ can be calculated by,

$$S_n(f_m) = \sum_{k=-\infty}^{\infty} |kV_k|^2 S_\phi(f_m - kf_o) \tag{2.13}$$

Now the single-sideband phase noise power spectral density can be computed by,

$$\left(\frac{N_o}{P_o}\right)_{f_m} = \frac{S_n(f_o + f_m)}{P_o} = \frac{S_n(f_o + f_m)}{2|V_1|^2} \tag{2.14}$$

where V_1 is the voltage amplitude of the fundamental of $v_o(t)$, which has been introduced to further define P_o, thus providing an opportunity for cancellation of variables.

Substituting (2.13) into (2.14) yields,

$$\left(\frac{N_o}{P_o}\right)_{f_m} = \sum_{k=-\infty}^{\infty} \frac{1}{2} \left|\frac{kV_k}{V_1}\right|^2 S_\phi(f_m - (k-1)f_o) \tag{2.15}$$

Assuming $S_\phi(f)$ decreases rapidly and that $f_m \ll f_o$, (2.15) can be approximated by,

$$\left(\frac{N_o}{P_o}\right)_{f_m} \approx \frac{1}{2} S_\phi(f_m) \tag{2.16}$$

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This relationship breaks down for mean-squared phase deviations of $\phi(t)$ in excess of $0.1\,\text{rad}^2$ as described in [11]. Consequently, for purposes of prevailing usage, the relationship is defined, as opposed to approximated, in [11] and thus (2.16) becomes,

$$\left(\frac{N_o}{P_o}\right)_{f_m} \equiv \frac{1}{2}S_{\phi}(f_m) \tag{2.17}$$

The important observation is that the single-sideband phase noise PSD is linearly related to the PSD $S_{\phi}(f)$. Again, the relationship has been defined by the IEEE standard [11], but it can also be derived as shown here.

Several different treatments of phase noise have been presented over the years and include linear time-invariant and linear time-varying approaches, the most well-known of which are [12-20]. In general, these approaches involve linearization of the oscillator system about the unperturbed solution and subsequent analysis of the linear system with perturbation assuming that the perturbation is small and bounded. These treatments, though useful, have been shown to contain incorrect assumptions and oversimplifications of the phase noise problem. For example, in [21], it has been shown that if the perturbation vector is a collection of uncorrelated white noise sources (an appropriate assumption for microelectronic oscillators), the variance of the solution to the system can grow unbounded. Moreover, artifacts of these approaches can be frustrating to reconcile in practice. For example, several of these approaches yield solutions that break down at small offset frequencies and evaluate to infinite power at the fundamental frequency.

In contrast to these approaches, a unified theory has been presented in [16] where the phase noise spectral density has been solved for an arbitrary oscillator. Specifically, in [16] it has been shown that the single-sideband phase noise PSD for an autonomous oscillator can be approximated by the Lorentzian function as follows,

$$\left(\frac{N_o}{P_o}\right)_{f_m} \approx \frac{f_o^2 c}{\pi^2 f_o^4 c^2 + f_m^2} \tag{2.18}$$

where c is a constant given by,

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$$c = \sum_{i=1}^{m} c_i \qquad (2.19)$$

and each c_i represents the noise contribution of the ith noise source of the m noise sources. Each c_i can be calculated as shown in [16].

The approximation in (2.18) is valid for $0 \le f_m \ll f_o$, and can be further approximated for $\pi f_o^2 c \ll f_m \ll f_o$ by,

$$\left(\frac{N_o}{P_o}\right)_{f_m} \approx \frac{c f_o^2}{f_m^2} \qquad (2.20)$$

It is obvious that the approximation given by (2.20) blows up as f_m approaches zero. In that case, (2.18) should be used and hence the corresponding bounds are placed on f_m for each expression. A more significant observation is that the phase noise expression in (2.18) is well-defined even at small offset frequencies.

The lower bound of (2.20) has significance and is commonly referred to as the corner frequency of the Lorentzian function in (2.18). This frequency is also known as the oscillator line width and is given by,

$$f_{lw} = \pi f_o^2 c \qquad (2.21)$$

It is obvious that expressions (2.18) and (2.20) characterize $1/f^2$ phase noise only. In [16] a solution was obtained by defining the phase deviation as a function of a perturbation vector. While performing the stochastic characterization of the phase deviation in [16], this vector was restricted to contain entries that represent white uncorrelated Gaussian noise. Thus, device flicker noise is not considered and flicker of frequency phase noise is not modeled. However, the authors in [16] have extended their work to account for colored noise sources in [18]. In this very rigorous approach, the stochastic characterization of $\phi(t)$ is found where $v_n(t) = v(t + \phi(t))$. Then the non-stationary autocovariance function of $v_n(t)$ is shown to be independent of time, t, for large t. The oscillator spectrum is then solved by taking the Fourier transform of the stationary autocovariance function of $v_n(t)$. To derive the solution, first define the Fourier coefficients of $v_n(t)$ by,

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$$v_n(t) = \sum_{k=-\infty}^{\infty} V_k e^{j2\pi k f_o t} \tag{2.22}$$

In [18], it has been shown that the spectral density of $v_n(t)$ for only colored noise sources can be found from the Fourier transform in the stationary autocovariance function for $v_n(t)$ which was determined to be,

$$S_{v_n}(f_m) = \sum_{i=-\infty}^{\infty} V_k V_k^* S_i(f_m + i f_o) \tag{2.23}$$

where $S_i(f)$ can be approximated by,

$$S_i(f_m) \approx i^2 |V_1|^2 \frac{f_o^2}{f_m^2} S_N(f_m) \tag{2.24}$$

for $fm \gg 0$ and where $S_N(f)$ is the spectral density of the colored noise source.

The authors in [18] continue by extending these results to the case of both white and colored noise sources in the system. The resulting form is identical to (2.23), where $S_i(f)$ is now defined by,

$$S_i(f_m) \approx i^2 \frac{f_o^2}{f_m^2} \left(c_w + \sum_{m=1}^{M} |V_{1m}|^2 S_{Nm}(f_m) \right) \tag{2.25}$$

for $f_m \gg 0$ and where M zero-mean, Gaussian, stationary, colored stochastic processes are considered and c_w is as defined in [18].

The spectrum that results from (2.23) where $S_i(f)$ is defined by (2.25) has the Lorentzian shape far from the fundamental and a shape of $1/f^2$ multiplied by the shape of the colored noise source for offset frequencies close to the fundamental. In the case of flicker noise, this results in a $1/f^3$ shape.

In [22], another analytical model including flicker noise has been developed. Specifically, this model utilizes the Lorentzian function for the device white noise sources and the Gaussian function for the device flicker noise sources. The final spectral representation is found from the convolution of the two functions. The result is the Voight line profile for

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which there is no analytical expression and results must be obtained numerically. These models, though analytically complete, lend little insight into the design aspects for low phase noise oscillators. However, for computer-aided design (CAD), these models are an excellent choice for accurate phase noise calculations.

At this point it is worthwhile to readdress the linearized models mentioned previously while taking a more circuit-specific approach to phase noise as some insight can be gained from these semi-empirical and analytical analyses. The classic linear time-invariant (LTI) approaches to phase noise include those presented in [12] and [13]. The treatment presented in [12] was one of the first published on the topic of phase noise and has been presented in detail in [13]. The derived phase noise density expression, commonly referred to as the Leeson model, in honor of the developer, is given by,

$$\left(\frac{N_o}{P_o}\right)_{f_m} = \frac{1}{8Q^2}\frac{FkT}{C}\left(\frac{f_o}{f_m}\right)^2 \tag{2.26}$$

where Q is the loaded quality factor of the reference, F is the noise factor (sometimes called the device excess noise number), k is Boltzmann's constant, C is the fundamental power, T is temperature, and the remaining terms are as defined previously. The concept of quality factor, or Q, will be addressed later within this chapter. The expression is useful in the sense that practical and physical relationships can be observed. These observations include the fact that increasing the quality factor and the fundamental power result in reduced phase noise. Correspondingly, temperature and noise factor increase the phase noise.

A semi-empirical modification to (2.26) has been presented in [23] where device flicker noise is considered. The derived expression, called the Leeson-Cutler model, is,

$$\left(\frac{N_o}{P_o}\right)_{f_m} = \frac{2FkT}{P_o}\left(1 + \left(\frac{f_o}{2Qf_m}\right)^2\right)\left(1 + \frac{f_{1/f^3}}{f_m}\right) \tag{2.27}$$

where f_{1/f^3} is the corner frequency between the $1/f^3$ and $1/f^2$ regions.

As described in [14], the most significant drawback associated with these two treatments of phase noise is that the parameter, F, is difficult to determine *a priori*. In fact, even in [12] it is mentioned that both F and f_{1/f^3} are usually fitted *a posteriori*. Moreover, the

treatment of flicker noise in (2.27) is completely empirical and thus has no physical foundation.

For the sake of completeness it is worth mentioning another popular LTI approach, which has been applied specifically to tuned inductor-capacitor, or LC, oscillators in [24]. Here the individual noise sources contributing to F have been identified and defined. The concept of an effective resistance or loss in the tank, R_{eff}, is introduced and defined by,

$$R_{eff} = R_L + R_C + \frac{1}{R_P(C\omega_o)^2} \qquad (2.28)$$

where R_L is the series loss in the inductor, R_C is the series loss in the capacitor, and R_P is the parallel loading caused by the sustaining amplifier.

Using this newly introduced concept of effective resistance, the phase noise spectral density can be defined by,

$$\left(\frac{N_o}{P_o}\right)_{f_m} = \frac{kTR_{eff}^2(1+A)(f_o/f_m)^2}{V_1^2/2} \qquad (2.29)$$

where A is a fitting parameter, V_1 is the amplitude of the fundamental, and flicker noise has not been modeled. Therefore, the improvement over the expressions in (2.26) and (2.27) is not substantial.

One of the most significant problems associated with an LTI approach to phase noise is that the noise in oscillators is typically cyclostationary. A cyclostationary random process, by definition, possesses bounded mean and variance that are periodic in time. Some intuition comes into play here. Consider that for most microelectronic oscillators, there is a period of time when the active device is conducting and another period of time where it is not. The device injects noise only when it is on and thus this noise injection is periodic. Although this argument is certainly not rigorous, if nothing else, it demonstrates that the process of noise injection is certainly time-varying.
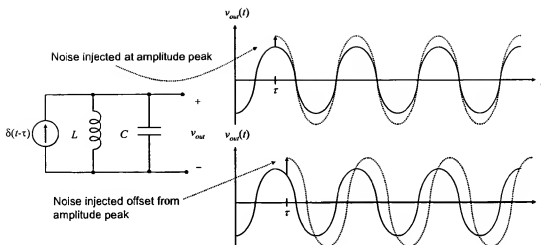
Figure 2.9 The time-varying nature of phase noise illustrated in an ideal *LC* network. Noise injected at an amplitude peak results in indefinite amplitude modulation while noise injected offset from an amplitude peak results in indefinite phase modulation [3].

Consider an ideal *LC* network as shown in Figure 2.9. Because the network is loss-less, any noise introduced into the circuit will be sustained infinitely. Now consider an impulse current that is injected into the circuit at some time τ, after the circuit has been in steady-state oscillation. Upon examination of Figure 2.9 it is clear that if the impulse occurs at an oscillation peak, the resulting signal becomes amplitude modulated. Thus, the output phase does not deviate from the initial phase, but the amplitude changes indefinitely. How-ever, if the impulse occurs some time between amplitude peaks, as shown, it is clear that the phase of the oscillation is perturbed indefinitely. Therefore, noise introduced while the output is in this portion of the cycle will contribute significantly to the phase noise, while noise introduced at the peaks of the oscillation will not contribute at all. The effect of noise on the behavior of the circuit is clearly time-varying.

An impulse sensitivity function (ISF), Γ(*t*), can be assigned to any oscillator topol-ogy. The ISF describes the time-domain regions where the oscillator is most sensitive to noise injection that will result in phase noise. Consider the output of an *LC* oscillator again. This topology is most sensitive to noise at the zero-crossings and least sensitive at the peaks, as illustrated by Figure 2.10. The corresponding ISF quantifies this concept. Math-ematically, the ISF is simply the phase impulse response. It is dimensionless and it quanti-

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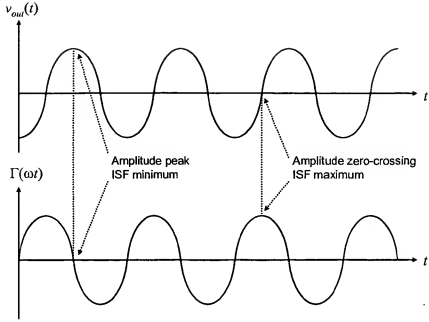
Figure 2.10   Time-domain voltage waveform of an ideal *LC* oscillator and the corresponding ISF indicating relative sensitivity to noise injection over time. Peaks in the oscillator time-domain waveform are immune to noise injection while maximum susceptibility to noise exists in the transition regions [14].

fies the amount of phase shift that results from injecting a unit impulse into the system and time $t = \tau$.

This linear time-varying (LTV) approach has been presented in [14] and is known commonly as the Hajimiri phase noise model, named after the developer. Although the LTV approach is rather insightful, a much more substantial contribution of the work is physical characterization of flicker noise. Here, a summary of this approach is presented.

In [14] a non-rigorous simulation-based technique is employed to justify the linearity of the analyzed system. Moreover, as described previously, it has been shown in [21] that linearization around the unperturbed solution, assuming a bounded perturbed solution, is incorrect because the solution can be shown to be unbounded. Nevertheless, the technique provides restrictions under which the system is linear.

The general approach, illustrated conceptually in Figure 2.11, begins with the assumption that the system is linear about the operating point and the system is time varying. The generalized concept is to characterize the system by its phase impulse response.

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The resulting response, due to an arbitrary noise source, is then injected into a nonlinear model for the system where upconversion of the flicker noise around the fundamental can be characterized. The noise is shaped by the ISF and thus this aspect comprises the time-varying component of the model.

The phase impulse response can be described by,

$$h_\phi(t, \tau) = \frac{\Gamma(\omega_o t)}{q_{max}} u(t - \tau) \tag{2.30}$$
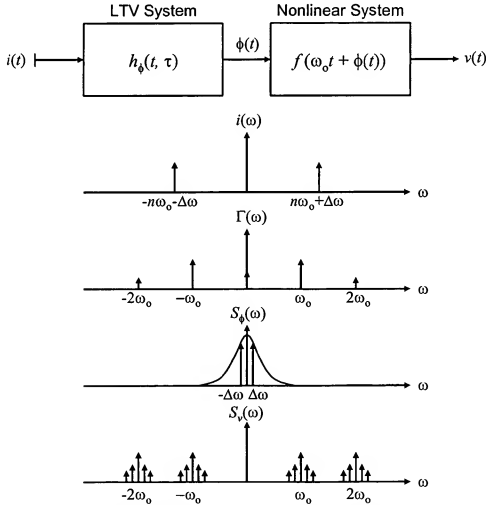
Figure 2.11 Hajimiri's LTV model for phase noise decomposed into LTV and nonlinear systems. Noise is passed through an LTV system and then injected into a nonlinear system to model frequency translation due to nonlinearity. The ISF shapes the noise and thus introduces the time-varying aspect of the model [14].

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where $u(t)$ is the unit impulse function, and q_{max} is the maximum charge displacement across the storage element (typically a capacitor) in the oscillator. The output phase is calculated by,

$$\phi(t) = \int_{\infty}^{-\infty} h_\phi(t, \tau) i(\tau) d\tau \qquad (2.31)$$

Using the fact that the ISF is periodic, it can be represented by a Fourier series,

$$\Gamma(\omega_o t) = \frac{c_o}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_o \tau + \theta_n) \qquad (2.32)$$

and thus $\phi(t)$ can be rewritten with a change of integration and summation,

$$\phi(t) = \frac{1}{q_{max}} \left[\frac{c_o}{2} \int_{-\infty}^{t} i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} \cos(n\omega_o \tau) d\tau \right] \qquad (2.33)$$

where the phase angle in (2.32) has been dropped because it is insignificant in the case of random noise injected into the system.

Consider a specialized case of $i(t)$ where,

$$i(t) = I_n \cos \Delta \omega t \qquad (2.34)$$

where I_n is the amplitude of $i(t)$ and $\Delta \omega \ll \omega_o$. In this case and under this condition, (2.33) can be approximated by,

$$\phi(t) \approx \frac{I_o c_o}{2 q_{max}} \int_{-\infty}^{t} \cos(\Delta \omega \tau) d\tau = \frac{I_o c_o \sin \Delta \omega t}{2 q_{max} \Delta \omega} \qquad (2.35)$$

Now consider a general case where,

$$i(t) = I_n \cos[(n\omega_o + \Delta \omega) t] \qquad (2.36)$$

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and where I_n is the amplitude of $i(t)$ and $\Delta\omega$ is a small offset from any integer multiple, n, of ω_o. The result in $S_\phi(\omega)$ will be sidebands at $\pm\Delta\omega$. Therefore, (2.33) can be approximated by,

$$\phi(t) \approx \frac{I_n c_n \sin\Delta\omega t}{2q_{max}\Delta\omega} \tag{2.37}$$

Consequently, injection of a current in the form of (2.36) will result in single-tone phase modulation with equal sidebands at $\omega_o \pm \Delta\omega$. This concept is also illustrated in Figure 2.11 where $i(\omega)$ contains spectral components at $n\omega_o \pm \Delta\omega$ which result in sidebands in $S_\phi(\omega)$ at $\pm\Delta\omega$.

Thus, as is shown in [14], the phase noise PSD can be computed for an arbitrary white noise source by projection of the PSD of that source, $\overline{i_n^2}/\Delta f$, onto all of the c_n coefficients.

$$\left(\frac{N_o}{P_o}\right)_{f_m} = 10\log\left(\frac{(\overline{i_n^2}/\Delta f)\sum_{n=0}^{\infty} c_n^2}{4q_{max}^2\Delta\omega^2}\right) \tag{2.38}$$

Using Parseval's relation,

$$\sum_{n=0}^{\infty} c_n^2 = \frac{1}{\pi}\int_0^{2\pi}|\Gamma(x)|^2 dx = 2\Gamma_{rms}^2 \tag{2.39}$$

where $\Gamma_{rms}(x)$ is the root-mean-square value of $\Gamma(x)$. Now (2.38) can be rewritten as,

$$\left(\frac{N_o}{P_o}\right)_{f_m} = 10\log\left(\frac{\Gamma_{rms}^2 \overline{i_n^2}/\Delta f}{q_{max}^2 2\Delta\omega^2}\right) \tag{2.40}$$

And thus a simple expression for the phase noise PSD is derived for an arbitrary noise source. The expression in (2.40) can be used to determine the noise contribution for each source, or more simply, one equivalent noise source.

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Now flicker noise can be introduced. Consider again the Fourier coefficients, c_n, of $\Gamma(t)$ and the fact that the nonlinear model accounts for mixing of noise to sidebands around the fundamental frequency, as shown in Figure 2.12. Clearly c_o is the only coefficient that contributes to the conversion of flicker noise around the fundamental frequency under the condition that $\omega_{1/f} << \omega_o$, where $\omega_{1/f}$ is the active device flicker noise corner frequency. Now consider a device flicker noise source of the form,

$$\overline{i_{n,\,1/f}^2} = \overline{i_n^2}\frac{\omega_{1/f}}{\Delta\omega} \tag{2.41}$$

By substituting (2.41) into (2.38) and accounting for only c_o, one obtains,

$$\left(\frac{N_o}{P_m}\right)_{\!o,\,f_m} = 10\log\left(\frac{c_o\,\overline{i_n^2}/\Delta f\omega_{1/f}}{q_{max}^2\,4\Delta\omega^2\,\Delta\omega}\right) \tag{2.42}$$

The breakpoint between the $1/f^2$ and $1/f^3$ region in the oscillator phase noise PSD is defined by the offset frequency at which the noise power contributed by the white noise
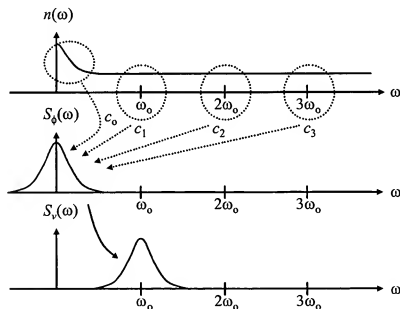
Figure 2.12   An arbitrary composite flicker and white noise source spectrum, $n(\omega)$, as it contributes to $S_\phi(\omega)$ and is ultimately translated around ω_o by nonlinearity in the system. The Fourier coefficients of $\Gamma(t)$ determine the magnitude of the phase noise that is contributed by noise at the respective frequencies [14].

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sources equals the noise power contributed by the $1/f$ sources. Call this break point, ω_{1/f^3}. It can be found by equating (2.40) and (2.42) and solving.

$$\omega_{1/f^3} = \omega_{1/f} \left(\frac{c_o}{2\Gamma_{rms}}\right)^2 \approx \omega_{1/f} \frac{1}{2}\left(\frac{c_o}{c_1}\right)^2 \qquad (2.43)$$

Clearly the oscillator corner frequency does not equal the flicker noise corner frequency of the active device unless $c_o/c_1 = \sqrt{2}$. Thus, a fascinating conclusion is that the close-in phase noise in an oscillator can actually be substantially less than the phase noise of the active device used in that oscillator.

The consequences of Hajimiri's analysis are nontrivial. Several design implications have been elaborated further in [14], but here it suffices to recall that the Fourier coefficients of the ISF, c_n, play a substantial role in the phase noise characterization of oscillators. In particular, c_o is responsible for flicker noise upconversion around the fundamental.

Below is a summary of the conclusions that can be drawn from Hajimiri's analysis. Many of these conclusions will be used later in the selection of an appropriate oscillator topology as well as in the design of that oscillator for the clock synthesizer in this work.

- The ISF and its associated time-varying properties of noise in oscillators play a significant role in the selection of oscillator topology. In particular, the Fourier coefficients of the ISF, c_n, are directly proportional to the phase noise and the ISF is directly related to the oscillator topology.

- Increasing charge displacement, q_{max}, will reduce the phase noise quadratically.

- c_n can be reduced, for even n, by designing for a 50% duty cycle because the ISF is periodic.

- The device flicker noise corner and the oscillator flicker noise corner do not necessarily match. The two approximately match only when $c_o/c_1 = \sqrt{2}$.

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• Flicker noise upconversion can be reduced by minimizing c_o. c_o can be reduced by increasing the waveform symmetry and by designing for equal waveform rise and fall times.

To conclude this subsection, it is worth noting that phase noise is a complicated process that has been approached in a variety of ways by several researchers. Some of these approaches are very useful in the design of electronic oscillators and many of the results found here will be employed later in the development of the clock synthesis system that is the focus of this work.

2.2.1.2 Jitter

It is important to begin by distinguishing between the two canonical forms of jitter: synchronous and accumulating. In some contexts, these forms of jitter are termed phase modulated (PM) and frequency modulated (FM) jitter respectively. Synchronous jitter is exhibited by driven systems, while accumulating jitter is exhibited by autonomous systems. Consider a simple D flip-flop driven by an ideal reference, where the output of the flip-flop is clearly a function of the input. The jitter produced at the output is a result of variations in the delay through the flip-flop from input to output. Variation can be due to no other effect because the input signal is ideal. Thus, the phase is perturbed from input to output and hence this type of jitter is termed PM jitter. Contrast this description to the concept of an autonomous oscillator. A transition in the oscillator output is based on its own previous transition. Thus the jitter is accumulating because each transition is referenced to the previous. Consequently, the frequency of the oscillator output varies in time and the phase of the oscillator output is unbounded. Thus, this form of jitter is often referred to as FM jitter. This work focusses on the jitter of autonomous oscillators for clock generation and thus, only accumulating, or FM, jitter will be addressed.

The simplest manner in which to describe time domain jitter is to rewrite (2.6) in the form,

$$v_n(t) = v(t + j(t)) \qquad (2.44)$$

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where $j(t)$ is the jitter. Here it is useful to define $\eta_T(t)$ as a T-cyclostationary stochastic process, which is stationary if sampled every T seconds. Recall that if $\eta_T(t)$ is T-cyclostationary then it must possess a bounded mean and variance that is periodic in T. Referring back to (2.44), for the case of synchronous jitter, $j(t) = \eta_T(t)$ and for accumulating jitter,

$$j(t) = \int_0^t \eta_T(\tau)d\tau \qquad (2.45)$$

If $\eta_T(t)$ is further restricted to be a white Gaussian T-cyclostationary process, then the exhibited PM and FM jitter are called simple PM and simple FM jitter respectively. In the case of simple FM jitter, if the process $j(t)$ is sampled every kT seconds for $k = \{1, 2, 3, \ldots\}$ then $\{j(kT)\}$ is a discrete Weiner process [25], a result which will be used later.

One could consider alternative restrictions on $\eta_T(t)$ in order to account for flicker noise. However, the variance of a flicker noise process is unbounded and thus the resulting process is not cyclostationary, which complicates the descriptions and analyses that follow. Of course flicker noise contributes significantly to the phase noise of an oscillator, particularly in CMOS. Nevertheless, including flicker noise in the descriptions and analysis that follow does not substantially improve any observations that are made or conclusions that are drawn. For now, it suffices to acknowledge that the noise sources have been restricted to being white, Gaussian, and T-cyclostationary.

The three most commonly employed timing jitter metrics for autonomous oscillators include long-term, period, and cycle-to-cycle jitter. All three metrics quantify the uncertainty in the oscillator period. Consider $v_o(t)$ again and define the fundamental oscillation period as $T = 2\pi/\omega_o$. Next, consider the noisy signal, $v_n(t)$. Define the absolute instant in time of the kth positive voltage transition of $v_n(t)$ as t_k and the period of the kth cycle as T_k. The expected value of the discrete random sequence T_k is $E[T_k] = T$ where $T_k = t_{k+1} - t_k$.

The long-term, or n-cycle, jitter can then be defined as,

$$J_n(k) = \sqrt{var(t_{k+n} - t_k)} \qquad (2.46)$$

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This metric measures the variation of the signal edges across n cycles. The period jitter, J, is simply a specialized case of the long-term jitter, where $n = 1$ as given by,

$$J_1(k) = \sqrt{var(t_{k+1} - t_k)} = \sqrt{var(T_k)} = J \qquad (2.47)$$

and clearly J is simply the standard deviation of a single period.

Lastly, cycle-to-cycle jitter measures the variation between adjacent periods as given by,

$$J_{cc}(k) = \sqrt{var(T_{k+1} - T_k)} \qquad (2.48)$$

It has been shown in [26] that if an oscillator exhibits simple accumulating jitter, then these metrics can be related by,

$$J_n = \sqrt{n}J \text{ and } J_{cc} = \sqrt{2}J \qquad (2.49)$$

the former of which is rather intuitive. Recall that in autonomous systems, each transition is relative to the previous and thus the variance accumulates. It is worth noting that the long-term jitter diverges with time. All of these relationships are summarized in Table 2.1. Additionally, each jitter metric is illustrated in Figure 2.13.

The period jitter is of most interest in the design of oscillators as it characterizes the short-term variation in each period from the mean. This metric is utilized in a variety of time-domain specifications, including timing budgets for microprocessors. A final impor-

Metric	Expression	Relationship to other metrics
Long-term	$J_n(k) = \sqrt{var(t_{k+n} - t_k)}$	$J = J_n/\sqrt{n}$ and $J_{cc} = \sqrt{2/n}J_n$
Period	$J = \sqrt{var(T_k)}$	$J_n = \sqrt{n}J$ and $J_{cc} = \sqrt{2}J$
Cycle-Cycle	$J_{cc}(k) = \sqrt{var(T_{k+1} - T_k)}$	$J_n = \sqrt{n/2}J_{cc}$ and $J = J_{cc}/\sqrt{2}$

Table 2.1 Summary of jitter metrics and their relationships.
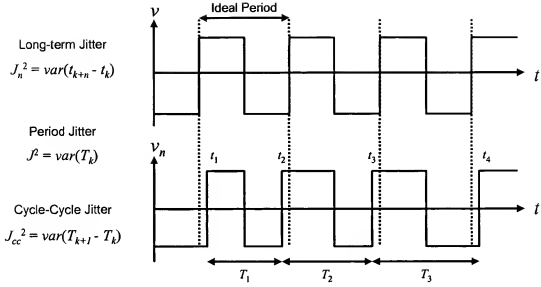
Figure 2.13 Jitter metrics illustrated. Each t_k indicates a positive rising edge of $v_n(t)$. Each T_k indicates the period designated by the difference between subsequent rising edges as given by $t_{k+1} - t_k$. Period jitter is of the most relevance to this work.

tant observation is that the period jitter, J, corresponds to the root-mean-square (RMS) jitter which is typically the metric specified in digital applications as well as the metric measured with time-domain instrumentation. This fact can be proven by consideration of the definition for each measure.

2.2.1.3 Allan Variance

Another common metric that measures the time-domain short-term stability of a periodic signal is the Allan variance, or two-sample deviation, named after the individual who developed the measure, David Allan. The Allan variance, as opposed to classical variance, converges for all natural noise processes and thus has been specified as one of the standards for characterizing short-term frequency stability [27]. In particular, the classical variance has been shown to diverge for random walk of frequency and flicker of frequency phase noise while the Allan variance does not [27]. Here the Allan variance is presented and defined as a specialized case of the classical variance. Begin by defining,

$$y(t) \equiv \frac{\phi(t)}{2\pi f_o} \qquad (2.50)$$

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where $\phi(t)$ is as in (2.6). Now define $\bar{y}_k$ by,

$$\bar{y}_k \equiv \frac{1}{\tau} \int_{t_k}^{t_k + \tau} y(t) dt = \frac{\phi(t_k + \tau) - \phi(t_k)}{2\pi f_o \tau} \qquad (2.51)$$

where $t_{k+1} = t_k + T$, $k = \{1, 2, 3, \dots\}$, and τ is the measurement duration which is repeated for every time T. Now define a frequency stability measure, σ_y^2, in terms of the classical N-sample variance,

$$\sigma_y^2(N, T, \tau) \equiv E\left[\frac{1}{N-1} \sum_{n=1}^{N} \left(\bar{y}_n - \frac{1}{N} \sum_{k=1}^{N} \bar{y}_k\right)^2\right] \qquad (2.52)$$

The Allan variance is a specialized case of (2.52) where $N = 2$ and $T = \tau$. It is also now clear from where the alternate terminology, the two-sample deviation, originates. The Allan variance is defined as,

$$\sigma_y^2(2, \tau, \tau) = \sigma_y^2(\tau) = \frac{1}{2} E[(\bar{y}_{k+1} - \bar{y}_k)^2] \qquad (2.53)$$

For a finite number of measurements, m, the Allan variance is computed by,

$$\sigma_y^2(\tau, m) = \frac{1}{m} \sum_{j=1}^{m} \frac{1}{2} (\bar{y}_{k+1} - \bar{y}_k)_j^2 \qquad (2.54)$$

The Allan variance, though a very useful metric, does not change with frequency translation, as will be shown in subsequent sections. It is presented here for completeness, but it will not be used as a short-term stability metric in this work.

2.2.1.4 Relationship Between Phase Noise and Jitter

Consider the noisy periodic signal, v_n, again as given by,

$$v_n(t) = v(t + j(t)) \qquad (2.55)$$

where $v(t)$ is a noise free harmonic signal as given by,

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$$v(t) = V_o \cos(\omega_o t) \qquad (2.56)$$

and $j(t)$ is assumed to exhibit simple FM jitter. Therefore,

$$j(t) = \int_0^t \eta(\tau) d\tau \qquad (2.57)$$

where η is a white Gaussian T-cyclostationary stochastic process and $j(t)$ is a Wiener process as described previously.

In this analysis, η is considered to be a white Gaussian process for simplification. Of course, in practical circuits the noise sources are pink due to flicker noise, but this will not be addressed because it unnecessarily complicates this analysis. Additionally, it is important to justify the cyclostationarity of η. Recall the intuitive discussion presented previously. Consider that in any oscillatory CMOS circuit, the devices are on during part of the oscillation cycle and off during the remainder. Thus, the noise process is inherently cyclostationary because the devices can only contribute noise when on and these devices are turned on periodically. Again, this is by no means a rigorous treatment of the process η, but at least this discussion provides some intuition into the behavior of η.

Because η is white, the double-sided noise PSD is given by,

$$S_\eta(\omega) = c \qquad (2.58)$$

where c is the constant associated with the Lorentzian function and given is in (2.19). Therefore the autocorrelation function of η is found easily using the fact that the autocorrelation function and PSD are Fourier transform pairs and η is white Gaussian and T-cyclostationary. Therefore,

$$R_\eta(t_1, t_2) = R_\eta(t_1 - t_2) = R_\eta(\tau) = \frac{1}{2\pi} \int_{-\infty}^{\infty} S_\eta(f) e^{j\omega\tau} d\omega = c\delta(\tau) \qquad (2.59)$$

where δ is the Kronecker delta function.

Now consider that $j(t)$ is a Wiener process and thus its autocorrelation function is,

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$$R_j(t_1, t_2) = a \cdot min(t_1, t_2) \tag{2.60}$$

Recall that the period jitter is standard deviation of one period and thus,

$$J = \sqrt{var(j(t+T)-j(t))} = \sqrt{E[(j(t+T)-j(t))^2]} \tag{2.61}$$

$$= \sqrt{E[j(t+T)^2 - 2j(t+T)j(t) + j(t)^2]} \tag{2.62}$$

$$= \sqrt{E[j(t+T)^2] - 2E[j(t+T)j(t)] + E[j(t)^2]} \tag{2.63}$$

$$= \sqrt{R_j(t+T, t+T) - 2R_j(t+T, t) + R_j(t, t)} \tag{2.64}$$

$$= \sqrt{c(t+T) - 2ct + ct} = \sqrt{cT} \tag{2.65}$$

Recall that in (2.20), c has already been related to the phase noise PSD for offset frequencies greater than the oscillator line width. Solving (2.20) for c gives,

$$c = \frac{f_m^2}{f_o^2} \left(\frac{N_o}{P_o} \right)_{f_m} \tag{2.66}$$

and thus the single sideband phase noise PSD can be related to the period jitter using (2.65) and (2.66).

$$J = \sqrt{\frac{f_m^2}{f_o^3} \left(\frac{N_o}{P_o} \right)_{f_m}} \tag{2.67}$$

Again, recall that this relationship has been derived in the absence of device flicker noise. Nevertheless, this expression is reasonably accurate for period jitter calculations, as will be shown, and it is significant to the derivation of frequency translation relationships that will be derived in the next chapter. The expression can be evaluated by selecting a frequency at which the phase noise density is measured that is well above the corner frequency of the Lorentzian function as given in (2.21) and well below f_o.

Another popular technique for converting phase noise to jitter involves integration of the phase noise spectrum over a given bandwidth as shown in [28] and [29]. To begin

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this analysis, recall the generalized expression for phase and amplitude noise in a periodic signal as given in (2.6) and presented again below, but with a change in the trigonometric function in order to simplify the analysis.

$$v_n(t) = [V_1 + \varepsilon(t)]\sin[\omega_o t + \phi(t)] \qquad (2.68)$$

Ignore the amplitude noise and consider two subsequent positive-slope zero-crossings of $v_n(t)$ at the time instants t_1 and t_2 where, $v_n(t_1) = v_n(t_2) = 0$. Using (2.68) it is clear that,

$$\omega_o t_1 + \phi(t_1) = 0 \text{ and } \omega_o t_2 + \phi(t_2) = 2\pi \qquad (2.69)$$

The difference between the two equations is simply 2π, as given by,

$$\omega_o(t_2 - t_1) + \phi(t_2) - \phi(t_1) = 2\pi \qquad (2.70)$$

and the difference between the two times is simply $T_o + \delta t$ where $T_o = f_o^{-1}$ and δt is some small offset due to that phase noise. Substituting into (2.70) yields,

$$\omega_o(T_o + \delta t) + \phi(t_2) - \phi(t_1) = 2\pi \qquad (2.71)$$

After rearranging, the following is obtained,

$$\delta t = \frac{1}{\omega_o}(\phi(t_1) - \phi(t_2)) \qquad (2.72)$$

Now the RMS value of δt can be determined by taking the expectation of the square of the expression in (2.72). This RMS value corresponds to the jitter, previously denoted J and thus, this notation is introduced again.

$$\delta t_{RMS}^2 = J^2 = \frac{1}{\omega_o^2}(E[\phi^2(t_1)] - 2E[\phi(t_1)\phi(t_2)] + E[\phi^2(t_2)]) \qquad (2.73)$$

Assume that $\phi(t)$ is stationary and thus the autocorrelation depends only on the time difference, $\tau = t_2 - t_1$. Recall that the autocorrelation function and the PSD of $\phi(t)$ are Fourier transform pairs and specifically,

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$$R_\phi(\tau) = \int_0^\infty S_\phi(f) \cos 2\pi f\tau \, df \qquad (2.74)$$

where the autocorrelation function of $\phi(t)$ is given by,

$$E[\phi(t_1)\phi(t_2)] = R_\phi(t_2 - t_1) = R_\phi(\tau) \qquad (2.75)$$

Using (2.74) and substituting into (2.73) yields,

$$J^2 = \frac{2}{\omega_o^2} \int_0^\infty S_\phi(f)(1 - \cos 2\pi f\tau) df = \frac{2}{\omega_o^2} \int_0^\infty S_\phi(f)(2\sin^2 \pi f\tau) df \qquad (2.76)$$

where the following trigonometric identity has been employed:

$$1 - \cos 2u = 2\sin^2 u \qquad (2.77)$$

Now substitute the definition of $S_\phi(f)$ as given in (2.17).

$$J = \sqrt{\frac{8}{\omega_o^2} \int_0^\infty \left(\frac{N_o}{P_o}\right) \frac{1}{f_m} \sin^2 \pi f\tau \, df} \qquad (2.78)$$

The expression in (2.78) can be used in order to determine the RMS jitter by simply integrating using the approximation $\tau = T_o$. However, this is not always practical because it is very difficult to measure and simulate the close-to-carrier phase noise accurately. Consequently, in many applications a jitter bandwidth is specified and then (2.78) can be evaluated by changing the integration limits in order to correspond to the designated bandwidth. For example, the clock jitter specification in the Synchronous Optical Network (SONET) communications protocol is determined by integration of the oscillator phase noise within a 12kHz to 20MHz bandwidth [30], corresponding to a frequency range over which it is rather easy to measure the phase noise. In fact, many phase noise measurement systems support integration of the measured phase noise over a specified band of interest. However, such measurements are not nearly as physical and complete as the result obtained from the expression derived in (2.78). Moreover, arbitrary integration of the phase noise density

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over a bandwidth of interest will not yield a jitter measure that is at all related to a wideband time-domain period jitter measurement. As shown in (2.78), period jitter is calculated by integration of a phase noise PSD shaped by a trigonometric function. Some recent publications, including [31], have indicated that the period jitter can be determined by simply integrating the phase noise. It is important to observe that these reports are incorrect. In fact, it is trivial to show that use of the expressions derived within [31] will yield wildly inaccurate results when compared to measurements. Integration of the phase noise PSD within a given bandwidth gives the total phase deviation within that band and has no equivalence to period jitter as defined here.

Lastly, it is worth comparing the two jitter-to-phase-noise conversion techniques presented within this section as there often seems to be a great deal of confusion associated with the relationship between these two expression. In fact, the expression in (2.67) is simply a specialized case of (2.78). The primary assumption employed in the derivation in (2.67) is that the phase noise PSD can be represented by a Lorentzian function, corresponding to only white of frequency phase noise. Assume that the region in which white of frequency phase noise is exhibited is at an offset above the oscillator line width. Thus, the phase noise PSD can be approximated by,

$$\left(\frac{N_o}{P_o}\right)_{f_m} \approx \frac{cf_o^2}{f_m^2} \tag{2.79}$$

which was presented previously in (2.20). Now substitute (2.79) into (2.78).

$$J = \sqrt{\frac{8}{\omega_o^2} \int_0^\infty \frac{cf_o^2}{f_m^2} \sin^2 \pi f_m \tau \, df_m} \tag{2.80}$$

Make a change of variables to $x = \pi f_m \tau$ and substitute,

$$J = \sqrt{\frac{8\pi}{4\pi^2 f_o^3} \int_0^\infty cf_o^2 \frac{\sin^2 x}{x^2} dx} = \sqrt{\frac{2c}{\pi f_o} \int_0^\infty \frac{\sin^2 x}{x^2} dx} = \sqrt{\frac{2c}{\pi f_o} \frac{\pi}{2}} = \sqrt{\frac{c}{f_o}} \tag{2.81}$$

which is identical to the expression in (2.65). Now by using (2.79) and solving for c, the expression in (2.81) can be determined in terms of the phase noise PSD,

$$ J = \sqrt{\frac{f_m^2}{f_o^3}\left(\frac{N_o}{P_o}\right)_{f_m}} \tag{2.82} $$

which is identical to the expression in (2.67). Thus, it has been shown that the expression in (2.67) is simply a specialized case of (2.78) in which the entire phase noise PSD is modeled by the Lorentzian function.

Based on this analysis, it appears that the expression in (2.78) is substantially more accurate than the expression in (2.67) because the former is not specialized. Certainly this is true, but as discussed previously, it is quite difficult to measure the close-to-carrier phase noise. However, this phase noise is not a great significance due to the shaping by the trigonometric function, which is near zero at frequency offsets close-to-carrier. Nevertheless, it is quite difficult to measure jitter in general, as will be shown in Chapter 5. The measurement equipment not only introduces jitter, but it also limits the bandwidth of the measured signal, thus underestimating the actual jitter. Additionally, these analyses have presented only the phase noise induced jitter. In fact, the total jitter that is measured includes jitter due to white noise within the measurement bandwidth. The expression in (2.78) does account for this noise because the upper integration limit is infinite, although in practice this limit is bounded by the measurement equipment. The expression in (2.67) does not account for this noise. This topic will be addressed further in the measurements section of this work.

2.2.1.5 Relationship Between Phase Noise and Allan Variance

The Allan variance can be computed from the phase noise density, a derivation which will be presented here and which has been presented previously in [27]. However, the phase noise density cannot be defined from the Allan variance. As shown in [32], the mapping from the domain of the spectrum to the domain of the Allan variance is not one-to-one and thus, the Allan variance cannot be inversely mapped to a spectrum.

Begin with classical N-sample variance as defined previously in (2.52), and presented here again in (2.83).

$$\sigma_y^2(N, T, \tau) \equiv E\left[\frac{1}{N-1}\sum_{n=1}^{N}\left(\bar{y}_n - \frac{1}{N}\sum_{k=1}^{N}\bar{y}_k\right)^2\right] \qquad (2.83)$$

Now expand (2.83),

$$\sigma_y^2(N, T, \tau) = \frac{1}{N-1}\left\{\sum_{n=1}^{N}E[\bar{y}_n^2] - \frac{1}{N}\sum_{i=1}^{N}\sum_{j=1}^{N}E[\bar{y}_i\bar{y}_j]\right\} \qquad (2.84)$$

$$\sigma_y^2(N, T, \tau) = \frac{1}{(N-1)\tau^2}\sum_{n=1}^{N}\int_{t_n}^{t_n+\tau}dt''\int_{t_n}^{t_n+\tau}E[y(t')y(t'')]dt' \qquad (2.85)$$

$$-\frac{1}{N(N-1)\tau^2}\sum_{i=1}^{N}\sum_{j=1}^{N}\int_{t_i}^{t_i+\tau}dt''\int_{t_j}^{t_j+\tau}E[y(t')y(t'')]dt'$$

Recall that the autocorrelation function and the power spectral density of $y(t)$ are Fourier transform pairs and specifically,

$$S_y(f) = 4\int_0^\infty R_y(\tau)\cos 2\pi f\tau d\tau \qquad (2.86)$$

$$R_y(\tau) = \int_0^\infty S_y(f)\cos 2\pi f\tau df \qquad (2.87)$$

where the autocorrelation function of $y(t)$ is given by,

$$E[y(t')y(t'')] = R_y(t''-t') = R_y(\tau) \qquad (2.88)$$

Substitute (2.86) and (2.87) into (2.85).

$$\sigma_y^2(N, T, \tau) = \frac{1}{(N-1)\tau^2}\sum_{n=1}^{N}\int_0^\infty S_y(f)df\int_{t_n}^{t_n+\tau}dt''\int_{t_n}^{t_n+\tau}\cos 2\pi f(t''-t')dt' \qquad (2.89)$$

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$$- \frac{1}{N(N-1)\tau^2} \sum_{i=1}^{N} \sum_{j=1}^{N} \int_0^\infty S_y(f) df \int_{t_i}^{t_i+\tau} dt'' \int_{t_j}^{t_j+\tau} \cos 2\pi f(t''-t') dt'$$

$$\sigma_y^2(N, T, \tau) = \frac{1}{(N-1)\tau^2} \sum_{n=1}^{N} \int_0^\infty S_y(f) \frac{(\sin \pi f \tau)^2}{(\pi f)^2} \tag{2.90}$$

$$- \frac{1}{N(N-1)\tau^2} \sum_{i=1}^{N} \sum_{j=1}^{N} \int_0^\infty \frac{S_y(f)}{(2\pi f)^2} df \times [2 \cos 2\pi f T(j-i)$$

$$- \cos[2\pi f T(j-i) + \tau] - \cos[2\pi f T(j-i) - \tau]]$$

Note that the first term of the expression above is a summation over n and is independent of n. Thus it will be reduced. Also, the following portion of the expression above may be reduced as follows,

$$2 \cos 2\pi f T(j-i) - \cos[2\pi f T(j-i) + \tau] - \cos[2\pi f T(j-i) - \tau] \tag{2.91}$$

$$= 4(\sin \pi f \tau)^2 \cos 2\pi f T(j-i)$$

With this simplification, the entire second term of (2.90) becomes,

$$- \frac{1}{N(N-1)\tau^2} \int_0^\infty \frac{S_y(f)}{(\pi f)^2} (\sin \pi f \tau)^2 df \sum_{i=1}^{N} \sum_{j=1}^{N} \cos 2\pi f T(j-i) \tag{2.92}$$

Now let $j - i = k$ and $2\pi f T = $. With this change of variables, the double summation in (2.92) becomes,

$$\sum_{i=1}^{N} \sum_{j=1}^{N} \cos 2\pi f T(j-i) = \sum_{i=1}^{N} \sum_{k=1-i}^{N-i} \cos kx \tag{2.93}$$

The summand in (2.93) is independent of i and thus the order of the summations may be interchanged. The summand is also even in k and thus the contributions are equal for $\pm k$. Finally, pulling out the $k = 0$ term and reducing (2.93) gives,

$$\sum_{i=1}^{N} \sum_{k=1-i}^{N-i} \cos kx = 2\left(\sum_{k=1}^{N-1} \cos kx \sum_{i=1}^{N-k} 1\right) + \sum_{i=1}^{N} 1 = 2\left(\sum_{k=1}^{N-1} (N-k)\cos kx\right) + N \qquad (2.94)$$

Now (2.94) may be rewritten as,

$$2\left(\sum_{k=1}^{N-1} (N-k)\cos kx\right) + N = N + 2Re\left[N - \frac{1}{i}\frac{d}{dx}\right]\sum_{i=1}^{N-1} e^{jkx} \qquad (2.95)$$

And (2.95) may be reduced as follows,

$$N + 2Re\left[N - \frac{1}{i}\frac{d}{dx}\right]\sum_{i=1}^{N-1} e^{jkx} = N + 2Re\left[\left\{N - \frac{1}{i}\frac{d}{dx}\right\}\frac{e^{jx} - e^{jNx}}{1 - e^{jx}}\right] \qquad (2.96)$$

$$= N + 2Re\left[\frac{1 - e^{jNx} - N(1 - e^{jx})}{4(\sin(x/2))^2}\right] \qquad (2.97)$$

$$= \frac{(\sin(Nx/2))^2}{(\sin(x/2))^2} \qquad (2.98)$$

Finally, define $r = T/\tau$ and substitute the expression in (2.98) into (2.92). The general expression then becomes,

$$\sigma_y^2(N, T, \tau) = \frac{N}{N-1} \int_0^\infty S_y(f) \frac{(\sin\pi f\tau)^2}{(\pi f\tau)^2}\left[1 - \frac{(\sin\pi r f N\tau)^2}{N^2(\sin\pi r f\tau)^2}\right] df \qquad (2.99)$$

And for the specific case of the Allan variance, $N = 2$ and $r = 1$ because $\tau = T$.

$$\sigma_y^2(\tau) = 2 \int_0^\infty S_y(f) \frac{(\sin\pi f\tau)^4}{(\pi f\tau)^2} df \qquad (2.100)$$

Here it is useful to relate $S_y(f)$ to $S_\phi(f)$. Recall that $y(t)$ was defined in (2.50) as,

$$y(t) \equiv \frac{\phi(t)}{2\pi f_o} \qquad (2.101)$$

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and thus, $y(t)$ and $\phi(t)$ have a simple scalar relationship. Now the relationship between the PSDs is given by,

$$S_y(f) = \left(\frac{1}{2\pi f_o}\right)^2 S_\phi(f) \qquad (2.102)$$

Recall that $S_\phi(f)$ has been related to $(N_o/P_o)_{f_m}$ by derivation and definition previously and specifically, $S_\phi(f_m)/2 = (N_o/P_o)_{f_m}$. The Allan variance can be written in terms of the single sideband phase noise PSD as,

$$\sigma_y^2(\tau) = \left(\frac{1}{2\pi f_o}\right)^2 \int_0^\infty \left(\frac{N_o}{P_o}\right)_{f_m} \frac{(\sin \pi f_m \tau)^4}{(\pi f_m \tau)^2} df_m \qquad (2.103)$$

This relationship has been derived independent of the noise statistics and thus the conversion in (2.103) is quite useful. However, this conversion, like the generalized jitter conversion expression in (2.78), also requires measurement of the close-to-carrier phase noise, which is difficult. For this reason, the analysis above is useful in order to determine the relationship between changes in the phase noise and the Allan variance. Beyond that, this measure will not be used.

2.2.2 Long-Term Frequency Stability

The long-term frequency stability characterizes the change in oscillation frequency over a long period of time, such as days or years. Long-term instability is commonly referred to as aging. Several environmental effects can lead to aging in harmonic oscillators. For example, any mechanical resonant device is subject to mass-loading, stress, and outgassing. Mass-loading is the random adsorption and desorption of environmental particles over a period of time. These particles change the effective mass of the resonant device and thus change the resonant frequency. Additionally, the stress in the material can change over time due to environmental temperature changes and thus the stiffness is affected, which in turn changes the resonant frequency of the device. Some materials, such as quartz, may have small pockets of gas trapped within them from manufacturing. These gasses are released over time and cause the resonant frequency to drift by mass-loading.
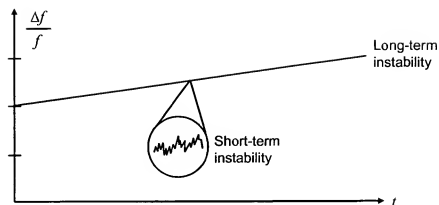
Figure 2.14   Short-term and long-term fractional frequency instability illustrated as a function of time.

The frequency deviation behavior of a typical oscillator is shown in Figure 2.14, where both long-term and short-term frequency instability are illustrated. As described, short-term instability can be quantified by jitter or phase noise. Long-term stability measures simply make use of the same metrics but over longer periods of time.

2.2.3 Rise/Fall Times and Symmetry

The basic electrical characteristics of the clock waveform are critical in many applications. For example, long rise and fall times in the clock signal cause excessive power dissipation in CMOS circuits due to short-circuit current draw in the clock transition region. Consider a simple CMOS inverter and recall that as the clock switches there exists a path through both nMOS and pMOS transistors between the power supply and ground. Substantial current can be drawn temporarily through this path. Thus, it is obviously desirable for the clock to possess short rise and fall times. Referring to Figure 2.15, the rise and fall times are typically defined as the time a signal takes to traverse from the 10% to 90% points of the peak-to-peak voltage. Let,

$$v_{pp} = v_{hi} - v_{lo} \tag{2.104}$$

be the amplitude, or peak-to-peak voltage, of the clock signal. Then the rise and fall times, t_r and t_f respectively, can be defined as shown in Figure 2.15.

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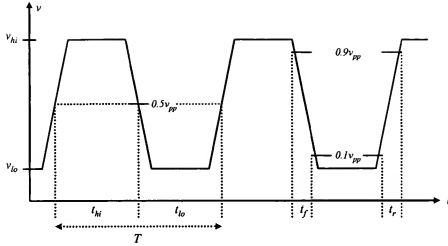
Figure 2.15 Waveform rise/fall times and symmetry illustrated. Rise/fall times are taken at the 90% and 10% amplitude positions. Symmetry is determined from the midpoints of the waveform.

In many embedded applications, both the rising and falling clock edges are used to transfer data. Thus, the waveform must be symmetric. Moreover, as has already been shown, waveform symmetry affects the short-term stability of an oscillator, so it is important that synthesized waveforms be symmetric.

The waveform high and low times are typically measured at the points at which the waveform is at 50% of the peak-to-peak voltage, as shown in Figure 2.15. The symmetry, or duty cycle, is then found from the ratio of the high and low times to the total period, or specifically, t_{hi}/T and t_{lo}/T where T is the period. Ideally, these ratios are equal to 0.5. This metric is also commonly referred to as the duty cycle and may be represented as a percentage, where the ideal is 50% for both the high and low times. In some cases an alternate duty cycle may be desired, particularly in the case of switched capacitor circuits, but clock signals such as these will not be addressed in this work.

2.2.4 Tuning Range

The tuning range, TR, is defined by,

$$TR = \frac{f_{max} - f_{min}}{f_{min}} \qquad (2.105)$$

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where f_{max} and f_{min} are the respective maximum and minimum frequencies that can be synthesized.

2.2.5 Frequency Accuracy

Frequency accuracy, A_f, is the measure of the frequency of the system as compared to an ideal reference. It is defined by,

$$A_f = \frac{f - f_r}{f_r} \tag{2.106}$$

where f is the output frequency of the system and f_r is the output frequency of a given reference. Accuracy can also be considered as the deviation around the mean frequency for a set of sample frequencies.

2.2.6 Power Supply Sensitivity

Power supply sensitivity is a measure of the change in oscillation frequency relative to variations in the power supply. This metric can be quantified with a generalized sensitivity function as follows,

$$S_{V_{DD}}^f = \frac{V_{DD}}{f} \frac{\partial f}{\partial V_{DD}} \tag{2.107}$$

where $S_{V_{DD}}^f$ is the power supply sensitivity, f is frequency, and V_{DD} is the power supply.

Analysis can be performed to determine the power supply sensitivity for any circuit topology. Consequently, circuit design techniques can be employed to increase the power supply stability. Moreover, the supply reference from which the circuit is biased plays a critical role in the power supply sensitivity.

2.2.7 Temperature Coefficient

The temperature coefficient measures the change in oscillation frequency over temperature. This metric can be quantified as follows,

$$TC_f = \frac{1}{f}\frac{\partial f}{\partial T} \tag{2.108}$$

where TC_f is the temperature coefficient, f is frequency and T is temperature. This metric is commonly reported in parts-per-million (ppm) and can be determined from analysis and test.

2.2.8 Microphonic Sensitivity

Microphonic sensitivity is a measure of the change in oscillation frequency relative to environmental vibration or acceleration. This metric can be quantified with a generalized sensitivity function as follows,

$$S_G^f = \frac{G}{f}\frac{\partial f}{\partial G} \tag{2.109}$$

where S_G^f is the microphonic sensitivity, f is frequency, and G is the vibration or acceleration force.

2.2.9 Frequency Settling Time

Often abrupt frequency changes in the clock signal are desirable. Consider a low-power embedded processor application where power is conserved by reducing the clock frequency. Often an external event will cause the processor to "wake-up" and thus the clock frequency is increased in order to manage the new processing demand. The time between the point when the event occurs and when the clock reaches the desired frequency can be be long for large frequency changes. In sensor applications where the external event is triggered by a signal that must be captured, this delay can be catastrophic because the event may be over before the processor reaches the desired frequency. PLLs have particularly long settling times for large frequency changes where the delay may be thousands of clock cycles. This settling time can be measured by simply measuring the time required to change between two distinct frequencies.

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2.2.10 System Metrics

Several system-related metrics should be considered in the development of a clock synthesis technology. These include size, cost, and power dissipation. These factors directly affect the selection of a clock synthesis technology in all applications. Generally speaking, all three should be minimized and thus the smallest, least-expensive, and lowest-power clock solution would be the best option for clock synthesis.

Several techniques for reducing power, cost, and size will be examined in further detail when the development of the clock synthesis system of this work is presented.

2.3 Oscillator Theory and Topologies

2.3.1 System Theory

In the most general sense, an oscillator is a positive-feedback network as shown in Figure 2.16. The associated transfer function is,

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 - G(s)H(s)} \tag{2.110}$$

where $G(s)$ is a frequency selection function describing the reference device and $H(s)$ describes the sustaining amplifier. Under the correct conditions, this positive-feedback network will be unstable and will oscillate. By inspection of (2.110), it is clear that the system
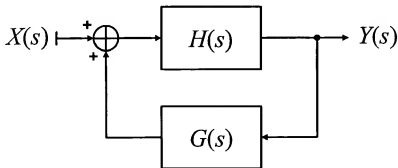
Figure 2.16   Frequency-domain system-level schematic of an oscillator as a positive-feedback network. $H(s)$ represents the sustaining amplifier and $G(s)$ represents the reference device.

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is unstable if $G(s)H(s)$ has a magnitude of 1 and a phase of 0°. These conditions are referred to as the Barkhausen criteria, which are stated mathematically in (2.111),

$$|G(s)H(s)| \geq 1 \text{ and } \angle G(s) + \angle H(s) = 0° \qquad (2.111)$$

where $G(s)H(s)$ is referred to as the loop gain, $T(s)$, and is given by,

$$T(s) = G(s)H(s) \qquad (2.112)$$

By solving the characteristic equation,

$$1 - T(s) = 0 \qquad (2.113)$$

one can find the location of the poles for this system. For an ideal reference, the solution to the characteristic equation will yield roots on the imaginary axis, as shown in Figure 2.17a. A practical reference will have loss and corresponding pole positions as shown in Figure 2.17b, the details of which are described later. The sustaining amplifier, $H(s)$, must compensate for the loss in order to maintain oscillation. In practice, the oscillator is designed such that the poles are in the right half plane (RHP), thus guaranteeing oscillation.

It should be noted that the Barkhausen criteria is necessary, but not sufficient for oscillation. In [33] it has been shown that it is possible for the Barkhausen criteria to be satisfied and yet the circuit will be stable.
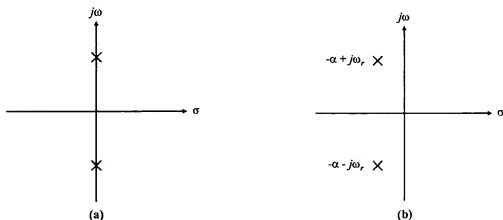
Figure 2.17 **Root locus diagram illustrating the pole positions of the natural frequencies of a harmonic oscillator. (a) Ideal oscillator. (b) Oscillator with loss.**

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2.3.2 Classification of Oscillators

2.3.2.1 Relaxation Oscillators

A relaxation oscillator, sometimes referred to as a multivibrator, is characterized by the presence of one equivalent storage element. Accompanying active circuitry is used to sense the state of that element and switch periodically. Figure 2.18 shows a schematic of a basic CMOS relaxation oscillator as presented in [19]. The matched pairs M_1 and M_2 act as switches that alternately charge the capacitor C. As shown in [19], the fundamental oscillation frequency for this circuit is given by,

$$\omega_o = \sqrt{\frac{g_m}{2RCC_D}} \tag{2.114}$$

where g_m is the small-signal transconductance of M_1 or M_2, R and C are as shown, and C_D is the capacitance at the drain of M_1 or M_2.

Relaxation oscillators are not nearly as accurate and stable as oscillator topologies from other classes such as the crystal oscillator, a type of harmonic oscillator. This is because the oscillation frequency is set by the transconductance of the active devices,
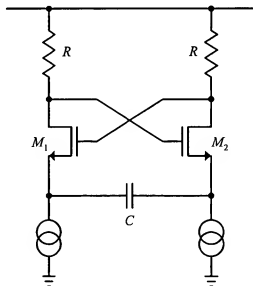
Figure 2.18   Basic CMOS relaxation oscillator. M_1 and M_2 switch alternately and charge C.

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which can vary significantly with process and bias conditions. Additionally, this type of oscillator has poor temperature stability due to the large temperature coefficient of integrated resistors. However, it is easier to integrate a relaxation oscillator than a harmonic oscillator because the storage element, often a capacitor, is typically available in modern CMOS process technologies. It is also substantially easier to tune a relaxation oscillator over a wide bandwidth as compared to a harmonic oscillator. For these reasons, some relaxation oscillators have appeared in commercial applications for clock and data recovery. However, it is difficult to achieve the stability and accuracy required for clock synthesis with a relaxation oscillator. This is relatively obvious given that the oscillation frequency is a function of the transconductance of the sustaining circuit, and the transconductance changes substantially with process variations, biasing conditions, and signal amplitude. Therefore, this oscillator class is not appropriate for this clock synthesis.

2.3.2.2 Ring Oscillators

A ring oscillator is a cascade of n delay elements, typically inverters, that are connected in a feedback loop as shown in Figure 2.19. For oscillation, n must be odd or, if n is even, a wire inversion must be introduced, which is possible only for differential delay elements. The oscillation frequency is set by the total delay around the loop as given by,

$$f_o = \frac{1}{2nt_d} \tag{2.115}$$

where t_d is the delay of a single stage.
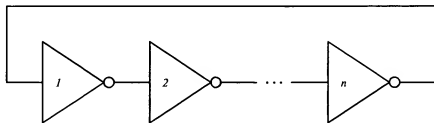
Figure 2.19   Basic n-stage inverter ring oscillator. Either n must be odd or, if n is even, a wire inversion must be introduced for the circuit to oscillate.

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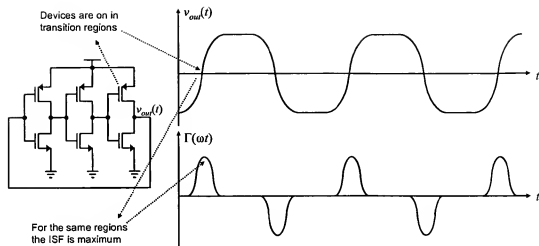
Figure 2.20   A 3-stage CMOS ring oscillator. The time-domain voltage output waveform is shown along with the corresponding ISF. For a CMOS ring oscillator, the devices draw current only in the transition region and therefore, noise is injected from the active devices in this region only. The transition region corresponds to an ISF maximum because noise introduced in these regions causes the most phase noise.

Ring oscillators are relatively common in microelectronic systems due to the fact that they are high frequency, easily tuned over a wide bandwidth, simple, low-power, and monolithic. However, ring oscillators are grossly inaccurate and unstable. Typically, a ring oscillator must be locked to a cleaner reference, such as a crystal reference, in order to improve accuracy and stability.

Here it is useful to recall Hajimiri's LTV phase noise model. Using the notion of the ISF, one can gain an intuitive understanding of the phase noise performance for a ring oscillator. Consider the basic ring oscillator topology as shown in Figure 2.20 where each stage is a simple CMOS inverter. The typical output of an oscillator is shown in Figure 2.20, along with the corresponding ISF. The ISF is maximized at the zero-crossings and minimized while the output is flat. Recall that injection of noise at an amplitude maximum or minimum does not introduce phase noise. However, noise injected in a transition region causes the maximum possible phase noise. Upon inspection of the ring oscillator circuit, it is clear that the output signal is flat when one of the devices is off and the other is operated in the linear region. While the devices are in these regions of operation, little noise is coupled to the output. However, while the signal is crossing zero, both devices are on and saturated. Here the potential for noise injection is maximized since it can originate from either

device or either supply rail. Unfortunately, this corresponds to the point at which the ISF function is maximized. Thus, this simple illustration clearly indicates the reason why ring oscillators exhibit such poor phase noise performance. Moreover, the design objective of a topology such as this one is to switch the devices as quickly as possible. Thus, the duration of time at which the ISF is non-zero is minimized.

The ring oscillator is not an appropriate class for clock synthesis, even though it is used in some low-performance and diagnostic applications. Despite the fact that it can be developed in monolithic form, with small size and low power, the instability and inaccuracy are typically not acceptable.

2.3.2.3 Phase-Shift Oscillators

A phase-shift oscillator is comprised of an active sustaining amplifier and a phase-shifting network so as to achieve 360° phase shift around the feedback loop, or equivalently 0°. Figure 2.21 illustrates a basic phase-shift oscillator with an inverting amplifier and RC network. At least three RC sections are required to achieve 180° phase shift because the phase shift for a single RC stage approaches 90° only as R approaches zero resistance. Of course, a voltage could not be developed across zero resistance to ground so the resistance must be finite, thus causing the maximum phase shift per stage to be less than 90°. Typically, a three-section oscillator is designed such that each section contributes a 60° phase shift. The sustaining amplifier gain must be at least equal to the inverse of the loss in the RC network
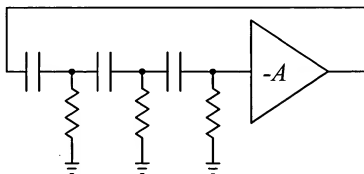
Figure 2.21 Basic phase-shift oscillator with inverting amplifier and 180° phase-shifting RC network. For matched RC components, each stage contributes 60° to the total phase shift. The inverting amplifier contributes the remaining 180°.

to ensure that the loop gain is equal to one. The circuit oscillates at the frequency for which the phase shift of the RC network is 180° given by,

$$\omega_o = \frac{\sqrt{6}}{RC} \tag{2.116}$$

Phase-shift oscillators can be integrated into a monolithic form because capacitor and resistor devices are available in modern CMOS process technologies. Tuning can also be achieved by varying the capacitance. However, the stability and accuracy performance of phase-shift oscillators is similar to that of relaxation oscillators. Therefore, these oscillators are not appropriate as a reference for clock generation. Nevertheless, some phase-shift oscillators can be found in the commercial market including a discrete clock generation component available form *MicroOscillator* [38], which is targeted at space and aviation applications because it is fully integrated in CMOS and contains no moving components, such as a crystal.

2.3.2.4 Harmonic Oscillators

Harmonic oscillators generate a periodic and sinusoidal signal form a reference that contains two equivalent storage elements operating in resonance. This resonance is detected and amplified by a sustaining feedback amplifier. A series or parallel inductor and capacitor pair, though electrical components, can represent any resonant device. Loss in the device can be modeled with the introduction of a series or parallel resistor. For mechanically resonant devices, such a quartz crystal, a current transformation analogy, as illustrated in Figure 2.22 and summarized in Table 2.3, can be employed. With this analogy, any resonant reference device, often referred to as a tank, can be represented ideally by an LC network. For mechanical references, the equivalent circuit is typically a series LC circuit, as shown in Figure 2.23a, and with loss as shown in Figure 2.23b. Electrically resonant tanks are typically parallel LC circuits as shown in Figure 2.23c, and with loss as shown in Figure 2.23d.

At this point, it is important to clarify what resonance. Electrical resonance is simply the condition under which the capacitive reactance and inductive reactance are of

Mechanical domain variable	Mechanical domain symbol	Electrical domain variable	Electrical domain symbol
Velocity	dx/dt	Current	i
Force	F	Voltage	v
Compliance	$1/k$	Capacitance	C
Damping	c	Resistance	R
Mass	m	Inductance	L

Table 2.2 Summary of relationships for the current electrical-mechanical analogy.
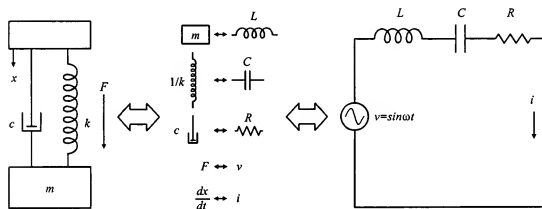
Figure 2.22   The electrical-mechanical analogy illustrated. The analogy shown is based on a current relationship where velocity in the mechanical domain is equivalent to current in the electrical domain.

equal magnitude. Under this condition, the tank will transfer energy between the two storage elements at a distinct frequency. The capacitor will discharge and induce a current in the inductor. The inductor then stores energy in a collapsing magnetic field that recharges the capacitor, which will again discharge and thus repeat the cycle. It is trivial to show that the natural resonant frequency for either LC network is $\omega_o = 1/\sqrt{LC}$ considering that by the definition of resonance presented, the reactances must be equal and thus $j\omega_o L = 1/j\omega_o C$. A more detailed analysis confirming this observation will be presented shortly.

Mechanical resonance is nearly identical to electrical resonance, and is exactly identical when the mechanical-electrical analogies are employed. Nevertheless, a more intuitive discussion of mechanical resonance is in order. Mechanical resonance is the con-

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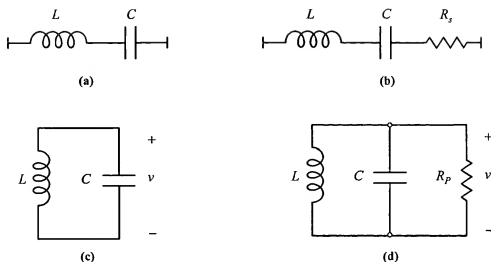
Figure 2.23 Electrical representations of a harmonic resonant reference device. (a) Ideal series LC tank. (b) Series tank with loss. (c) Ideal parallel LC tank. (d) Parallel tank with loss.

dition under which a disturbing force exactly coincides with the free vibration of the system [34]. At mechanical resonance, such a disturbing force causes vibration magnification, which continues indefinitely unless nonlinearity or loss exist in the system. The solution to a harmonic mechanically resonant system is identical to the electrical case, with only a substitution of variables by analogy, and several analogies exist.

The impedance presented by the tank circuit will appear differently depending upon whether the tank is a series or parallel resonant circuit. In the ideal case, a parallel LC tank will present infinite impedance at the resonant frequency while a series LC tank will present zero impedance. Considering loss, the parallel tank will present an impedance maximum, while the series tank will present an impedance minimum. Correspondingly there exist some variations in the nomenclature pertaining to resonance. Parallel resonance is often referred to as anti-resonant while the term resonance is reserved for series resonance. In this work, the term resonance will simply refer to the condition under which the inductive and capacitive reactive magnitudes are equal.

Both frequency and time-domain techniques can be employed to determine the natural frequencies of the harmonic system with either a series or parallel tank. Here analysis of the parallel system is performed, though it is trivial to obtain similar results from analysis

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of the series network. By applying Kirchoff's current law for the ideal case in Figure 2.23c one obtains,

$$C\frac{dv}{dt} + \frac{1}{L}\int_0^t vdt = 0$$ (2.117)

which can be reduced to,

$$\frac{d^2v}{dt^2} + \frac{1}{LC}v = \frac{d^2v}{dt^2} + \omega_o^2 v = 0$$ (2.118)

where

$$\omega_o = \frac{1}{\sqrt{LC}}$$ (2.119)

The characteristic equation of the system as given in (2.118) is a second order differential equation with solution,

$$v(t) = V_1 e^{j\omega_o t} + V_2 e^{-j\omega_o t} = V\cos\omega_o t$$ (2.120)

where V_1, V_2, and V are constants, the phase angle is zero by appropriate selection of the time origin, ω_o is the natural frequency of the system and the response is clearly harmonic.

The analysis can also be conducted by accounting for the loss in the reference device. By applying Kirchoff's current law again to the circuit in Figure 2.23d one obtains,

$$C\frac{dv}{dt} + \frac{v}{R} + \frac{1}{L}\int_0^t vdt = 0$$ (2.121)

which can be reduced to

$$\frac{d^2v}{dt^2} + \frac{1}{RC}\frac{dv}{dt} + \frac{1}{LC}v = \frac{d^2v}{dt^2} + 2\alpha\frac{dv}{dt} + \omega_o^2 v = 0$$ (2.122)

where

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$$\alpha = \frac{1}{2RC} \tag{2.123}$$

The solution to (2.122) can take one of three forms depending on the values of α and ω_o:

- Underdamped, where $\alpha < \omega_0$

- Critically damped, where $\alpha = \omega_0$

- Overdamped, where $\alpha > \omega_0$

In any practical harmonic resonant circuit, the response will be underdamped and have poles in the LHP. Thus the solution takes (2.122) the form,

$$v(t) = Ve^{-\alpha t}\cos\omega_r t \tag{2.124}$$

where the time origin has again been selected to produce a zero phase angle and,

$$\omega_r = \sqrt{\omega_o^2 - \alpha^2} \tag{2.125}$$

Clearly the presence of loss in the system causes the sinusoidal output to decay and thus a sustaining amplifier is required to maintain the oscillation. This phenomenon is called frequency pulling due to loss and a sample time-domain response is illustrated in Figure 2.24.

A frequency-domain approach can be employed to obtain identical results. Consider the ideal resonant tank and apply Kirchoff's law in the frequency-domain.

$$\frac{V}{sL} + sCV = 0 \tag{2.126}$$

which reduces to,

$$s^2 + \omega_o^2 = 0 \tag{2.127}$$

where the natural frequencies of the system are $\pm j\omega_0$ and correspond to the result from the time-domain analysis. Considering loss, the expression becomes,

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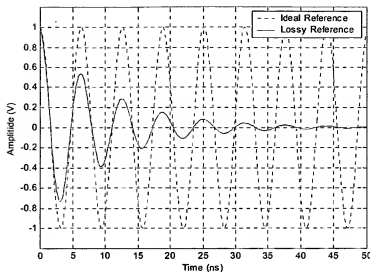
Figure 2.24   Ideal and underdamped response of a harmonic resonant reference.

$$\frac{V}{sL} + \frac{V}{R} + sCV = 0 \text{ or } s^2 + 2\alpha s + \omega_o^2 = 0 \qquad (2.128)$$

and the roots of this equation are,

$$s_1, s_2 = -\alpha \pm j\sqrt{\omega_o^2 - \alpha^2} = -\alpha + j\omega_r \qquad (2.129)$$

so the actual oscillation frequency is,

$$\omega_r = \sqrt{\omega_o^2 - \alpha^2} \qquad (2.130)$$

which also matches the time-domain analysis and the system theory presented previously.

At this point it is worthwhile to consider a root locus diagram for a practical oscillator. The oscillator will also contribute loss to the system due to loading and thus the total system loss, R, is the loss of the reference in parallel with the loading of the sustaining amplifier. However, the sustaining amplifier serves the function of pushing the poles into the RHP as illustrated in Figure 2.25, thus ensuring oscillation. In the steady-state, the poles settle on the $j\omega$ axis as illustrated. Consequently, the actual oscillation frequency differs from the oscillation frequency of the reference without loss. This oscillation frequency can

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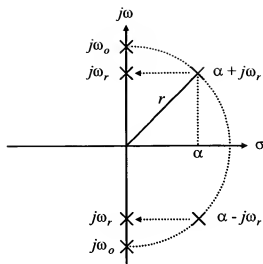
Figure 2.25 Root locus diagram of a practical oscillator. The poles are positioned in the RHP by overdesigning for the loss in the reference. In steady-state, the poles are pushed back onto the $j\omega$ axis. The actual resonant frequency, ω_r, thus differs from the natural resonant frequency.

be determined by geometric analysis. Referring to Figure 2.25, the following expression can be written for the geometry of the right triangle formed by the radius of the circle and the pole positions.

$$\omega_r^2 + \alpha^2 = \omega_o^2 \qquad (2.131)$$

Using (2.131), the actual oscillation frequency is $\omega_r = \sqrt{\omega_o^2 - \alpha^2}$, which is identical to the expression in (2.130). However, it is important to note that in (2.130), the system loss is due to the loss in the reference only, while in (2.131) the system loss is due to the parallel combination of the loss in the reference and the loading of the amplifier. Additionally, in the former case, α is positive and thus the poles are in the LHP and in the latter case, α is negative, which positions the poles in the RHP.

The vast majority of reference oscillators are harmonic oscillators. These oscillators typically exhibit the best frequency stability and accuracy. However, the performance of harmonic oscillators can vary greatly. For example, crystal oscillators are highly stable and accurate, while LC oscillators are much less accurate by comparison. However, crystals are typically trimmed in order to achieve high frequency accuracy. Nevertheless, LC oscillators can be tuned over a much wider bandwidth than crystal oscillators, which cannot be tuned

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at all. Some recently published micromechanical resonators can be tuned to some degree while providing stability comparable to crystal references [9]. However, these devices are still not nearly as accurate as crystal references.

Here again it is useful to recall Hajimiri's LTV phase noise model. The previous discussion has made clear that an ideal oscillator topology would cause noise injection at the ISF minimum and no injection at the ISF maximum. Many harmonic configurations actually approach this performance. For example, the Colpitts configuration (which will be discussed later), the corresponding tank voltage, and drain current are shown in Figure 2.26. Here the active device injects the maximum current at the voltage minimum, which corresponds to points where the ISF is low. As the voltage transitions from low to high, the active device begins to turn off. Therefore, the device is mostly off through the transition region. The phase noise performance of the Colpitts configuration is known to be very good. Although this is simply a qualitative discussion of the performance, it has been quantified and confirmed in previous work [35].

Research in the area of harmonic oscillators has increased substantially over the past several years, particularly with the advent of advanced communication systems requir-
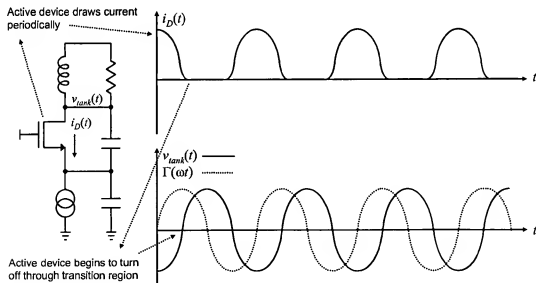
Figure 2.26 **Time-domain current and voltage waveforms for a CMOS Colpitts *LC* oscillator. The active device draws current periodically. As the tank voltage transitions from low to high, the active device begins to turn off. Therefore, the device is mostly off through the transition region where the ISF is at a maximum.**

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ing frequency synthesis for RF carriers. Embedded processor systems now also use several harmonic crystal-based oscillators as timing references for clocking. Much of the current research has been focused on developing new reference resonant devices, improving existing devices, achieving monolithic integration, improving circuit design techniques for achieving high-performance frequency synthesis, and understanding the noise processes that contribute to frequency instability. The harmonic oscillator is currently the best choice and the most likely candidate for monolithic clock synthesis. Therefore, the work presented in this dissertation is focused on this oscillator class.

2.3.3 Quality Factor of a Resonant Device

The notion of loss in the harmonic reference device was presented generally in the previous section and its effect on the oscillator performance, as compared to the ideal, was derived. A significant metric pertaining to this loss is the quality factor, or Q. The quality factor is a measure of the loss in any resonant system, as given by,

$$Q = 2\pi \frac{E_s}{E_d} \tag{2.132}$$

where E_s is the maximum instantaneous stored energy at resonance and E_d is the energy dissipated per cycle. Thus, an ideal resonant system has no energy dissipated, and infinite Q. Such a system would resonate at a single distinct frequency for an infinite length of time given any external excitation. This would be the ideal reference. Unfortunately no such reference exists. Nevertheless, the goal in reference development is to approach this ideal.

A more common expression for the Q-factor of electrical circuits is [36],

$$Q = \frac{\omega_o}{\Delta\omega} \tag{2.133}$$

where ω_o is the resonant frequency and $\Delta\omega$ is the 3dB bandwidth of the magnitude response for the tank. This notion of quality factor is illustrated in Figure 2.27. Here the magnitude response of an RLC network is plotted for three different Q-factors. The highest Q has the narrowest response.

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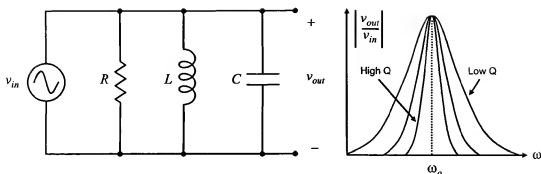
Figure 2.27 *Q*-factor illustrated. High-*Q* systems exhibit a narrow–band response.

It can be shown that the Q of a parallel RLC network is given by [37],

$$Q_p = \frac{R}{\omega L} \tag{2.134}$$

For a series RLC circuit, the Q is given by [37],

$$Q_s = \frac{\omega L}{R} \tag{2.135}$$

One must also consider the effect of the sustaining amplifier on the Q of the system. Typically this is referred to as the in-circuit-Q or loaded-Q. Consider Figure 2.28 where R_l represents the load of the active circuitry, R_s represents the loss in the series resonant device, and R_p represents the loss in the parallel resonant device. The loaded-Q is then given by,

$$Q_{ls} = \frac{\omega L}{R_s + R_l} \tag{2.136}$$

$$Q_{lp} = \frac{R_p \parallel R_l}{\omega L} \tag{2.137}$$

where Q_{ls} is the loaded-Q of the series tank and Q_{lp} is the loaded-Q of the parallel tank. Thus it is clear that the loading caused by the sustaining amplifier must be considered in the design of the reference oscillator. Discussing only the resonant device Q is insufficient. Clearly, design constraints surround the sustaining amplifier in order to minimize the load-

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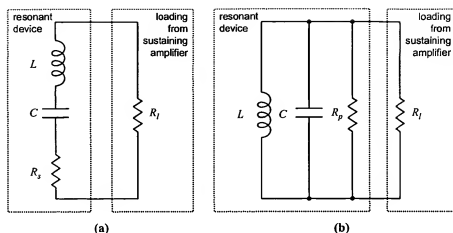
Figure 2.28 Loaded-Q of a resonant device illustrated. (a) Loading as a series resistor. (b) Loading as a parallel resistor.

ing, and these design constraints are not identical for the series and parallel tank, as can be seen by inspection of (2.136) and (2.137).

2.3.4 Harmonic Oscillator Models

2.3.4.1 Feedback Model

The generalized oscillator feedback system (presented previously in Figure 2.16), can be applied more specifically to the harmonic oscillator, as shown in Figure 2.29. Here $H(s)$ is the transfer function of the sustaining amplifier and $G(s)$ is the transfer function of the resonant device. As mentioned previously, $G(s)$ is commonly referred to as the tank. The tank performs the function of shaping the noise around the associated resonant frequency. The transconductance amplifier senses the tank voltage and delivers current back into the tank in order to sustain oscillation. The Barkhausen criteria, described previously, can be applied directly to this system. With a substitution of variables, the loop gain requirement becomes,

$$G_M R_P \geq 1 \tag{2.138}$$

and the phase requirement is, of course, the same.
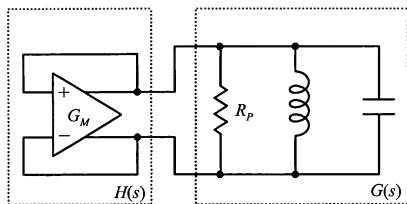
Figure 2.29 Positive feedback model for the harmonic oscillator including sustaining amplifier and resonant device represented by an *RLC* network.

2.3.4.2 Negative Resistance Model

Harmonic oscillators can also be described using a negative resistance model, sometimes also referred to as the negative-g_m model since the sustaining amplifier is typically a transconductance amplifier. Consider a resonant device, as a parallel *RLC* circuit, shown in Fig. 2.30 where R_P represents the loss in the device. If an impulse drives this network, the response will be a damped oscillation, which is entirely due to the loss component, R_P. Suppose there is a manner in which a negative loss could be introduced into the circuit and thus cancel the loss associated with the tank. In Figure 2.30 a negative resistance is introduced in parallel with R_P and the response to an impulse is illustrated, where the oscillation continues indefinitely.

It is possible to generate this negative-resistance using active components, as will be shown. If the introduced negative-resistance is exactly equal in magnitude to the loss resistor, R_P, then oscillation is guaranteed. In practice, the sustaining amplifier is designed such that the magnitude of the negative resistance is less than the loss component R_P, thus ensuring that the total parallel resistance is negative and thus the poles of the system are in the RHP. Throughout the oscillator start-up transient, the transconductance of the amplifier will then adjust such that R_P is cancelled exactly, after which the steady- state condition persists. Thus, in order to guarantee start-up, the following condition must hold,

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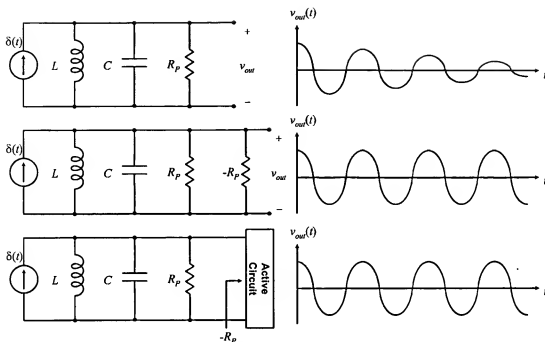
Figure 2.30   The concept of negative resistance illustrated. Due to loss, the network impulse response is damped as shown. If a negative resistance could be introduced that exactly cancels the loss, the oscillation could be sustained. Active electronics can be used to generate this negative resistance.

$$|R_{amp}| \leq |R_P| \qquad (2.139)$$

where $|R_{amp}|$ is the magnitude of the negative resistance generated by the active circuit.

It will be shown how this expression translates into a specification for the transconductance amplifier in a subsequent chapter that focuses on the design of the clock synthesis system in this work.

2.3.5 Harmonic Oscillator Topologies

Several oscillator topologies have been developed and presented over the years. Here only harmonic oscillator topologies are presented as this class of oscillators has been selected in the development of this work. In the sections that follow, only the most popular and relevant harmonic topologies are discussed including the Pierce, Colpitts, Hartley, cross-coupled, and complementary cross-coupled configurations.

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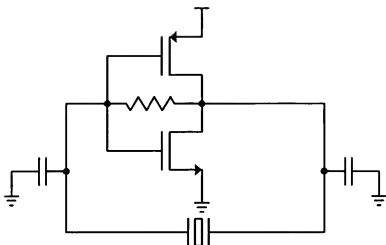
Figure 2.31 A CMOS Pierce crystal oscillator. The load is primarily reactive, thus providing high in-circuit Q and consequently good short-term stability.

2.3.5.1 Pierce

An implementation of the Pierce oscillator is shown in Figure 2.31. The Pierce topology is well-known because it provides excellent short-term frequency stability, primarily because the load on the tank is mostly capacitance and thus the in-circuit Q is very high. It is the most common topology for crystal-based references that interface with CMOS electronics because the oscillator can be implemented with only an inverter, a feedback resistor, two shunt capacitors, and the reference device. The Pierce topology is characterized by the fact that the reference device must present an inductive reactance in order for oscillation to occur. Thus, the inherent advantage in using this topology is that additional inductors are not required. However, the required external reactance is often quite large and thus in many cases the capacitors cannot be integrated.

2.3.5.2 Colpitts and Hartley

One LC implementation of the Colpitts oscillator is shown in Figure 2.32a. The circuit is characterized by a tapped capacitive feedback network around a single active device. Here the feedback network is shown from drain to source. Another configuration is possible where feedback is applied from the source to the gate. Both configurations are capable of

providing the positive feedback required for oscillation. Modifications to the Colpitts configuration also exist, such as the Clapp oscillator (not shown). The Clapp oscillator is simply a modified Colpitts oscillator where an extra capacitive tap is introduced. The extra tap allows the voltage swing across the inductor to be larger than would be with a simple Colpitts configuration. This is, of course, desirable because the phase noise can be reduced with increased signal power.

The Hartley configuration, shown in Figure 2.32b, is identical to the Colpitts configuration except that the inductor and capacitor positions are switched and thus the inductor is tapped, rather than the capacitor. The Hartley configuration is of more historical than practical significance. In the early days of RF electronics, tapped inductors were more readily available than tapped capacitors. In the modern world of integrated microelectronics, the tapped capacitor is more practical due to size considerations.

Both the Colpitts and Hartley oscillators can also be developed with a crystal reference and both exhibit excellent frequency stability characteristics. However, both an inductor and capacitor are still required in addition to the reference, thus making these configurations unattractive for monolithic integration. Nevertheless, the Colpitts configuration is still commonly found in microelectronic applications.

(a)   (b)
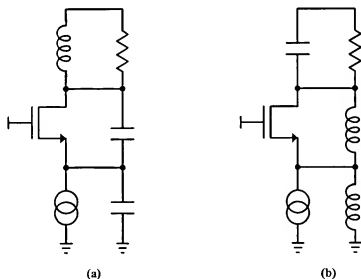
Figure 2.32   Common harmonic oscillator topologies. (a) Colpitts oscillator in an LC implementation. (b) Hartley oscillator as a dual of the Colpitts LC implementation.

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2.3.5.3 Cross-Coupled and Complementary Cross-Coupled

Previously it was shown that waveform symmetry can reduce flicker noise upconversion around the oscillation frequency. The cross-coupled configuration, shown in Figure 2.33a, is a balanced configuration that promotes waveform symmetry, thus reducing flicker noise upconversion. This topology is often referred to as a negative resistance topology because a negative resistance is generated across the drains of the nMOS devices.

An improved topology that possesses both top-bottom and left-right symmetry is shown in Figure 2.33b. This topology contains three specific advantages over the all-nMOS topology presented in Figure 2.33a. First, the increased symmetry of the circuit further promotes waveform symmetry. Second, the negative resistance generated in this topology is twice that of the all-nMOS topology and thus power can be reduced while an identical negative resistance is achieved. Third, the pMOS tail current introduces typically around one-tenth of the flicker noise that the nMOS tail current introduces. This is due to the fact that pMOS devices are typically buried channel devices in modern CMOS processes whereas

(a)   (b)
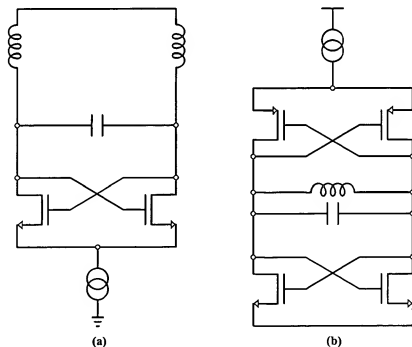
Figure 2.33   Negative resistance oscillator topologies that promote waveform symmetry. (a) Cross-coupled topology. (b) Complementary cross-coupled topology.

nMOS devices are typically surface channel devices. Consequently, the charge carriers in nMOS devices exhibit substantially higher flicker noise compared to pMOS, due to exposure to the silicon-gate-oxide interface.

The complementary cross-coupled configuration has been selected for this work because it is simple to integrate and the topology provides good frequency stability.

2.4 State-of-the-Art for Clock Generation

Three distinct implementations of clock synthesizers exist. They are discrete, hybrid, and monolithic. Also, two distinct frequency synthesis approaches exist and include PLL/DLL synthesized clock generation and free-running frequency synthesizers. The PLL/DLL approach is a frequency locking approach that typically involves locking a high-frequency voltage controlled oscillator (VCO) to a low-frequency crystal. Free-running oscillators do not lock to any reference other than the reference used for oscillation. The ubiquitous approach to clock generation is a hybrid implementation of a PLL/DLL synthesizer. However, free-running clock generation is appearing more commonly in low-end microcontroller applications and as discrete components themselves. In the sections that follow the state-of-the-art for clock generation is explored by implementation.

2.4.1 Discrete

A discrete PLL/DLL clock synthesizer is self-contained within a single package, where the only input signals are for programming and power and the only output signal is the clock. A diagram of an *Epson* SG-8002DC programmable clock synthesizer is shown in Figure 2.34. This device uses a crystal reference along with CMOS circuitry for a sustaining amplifier and a programmable PLL, all of which are contained within the package. The system is very simple to use given that it is self-contained and it provides excellent clock stability and accuracy, provided by the crystal reference.

The most significant drawbacks associated with this approach include size and power dissipation. The dual in-line package (DIP) shown in Figure 2.34 measures 13.7x6.6x5.3mm (LxWxH), which is larger than many 8-bit microcontrollers. Addition-

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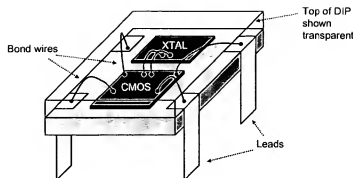
Figure 2.34 Diagram of an *Epson* SG-8002DC programmable discrete crystal-based clock synthesizer in a dual in-line package (DIP). The oscillator contains a complete PLL and crystal reference and can synthesize signals from 1 to 125MHz.

ally, at 3.3V the power dissipation is 92.4mW and at 5V it is 225mW. This level of power dissipation is unreasonable for any low-power processor, particularly if deployed in a portable application. The majority of the power dissipation comes from the PLL and the fact that a relatively high-frequency signal must be driven off-chip, through the package, and to the microprocessor or microcontroller that is being supported.

As for free-running oscillators, *MicroOscillator* has recently released a discrete CMOS clock product, the MOI-2000 [38], that uses a phase-shift oscillator topology [39]. Similar to the *Epson* product, the MOI-2000 is relatively expensive and large, mostly due to the discrete implementation. Of course, in contrast to the *Epson* approach, the MOI-2000 could certainly be integrated with a processor or any other CMOS electronics for that matter. However, the primary drawback associated with this approach is that the phase-shift oscillator does not exhibit good frequency accuracy and stability performance. For example the MOI-2000 is a temperature compensated component that exhibits ±0.5% frequency variation over the temperature range from 0-70°C. It will be shown that the approach developed in this work achieves better temperature performance over a larger frequency range and without any compensation.

2.4.2 Hybrid

Hybrid PLL/DLL clock synthesis is the ubiquitous technique used in modern microelectronic systems. In fact, nearly every single embedded microcontroller or microprocessor
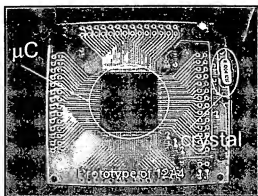
Figure 2.35 *Motorola's* MC68HC812A4 microcontroller mocked-up on a PC board. The discrete crystal interfaces with an on-chip sustaining amplifier, which together comprise the reference oscillator. This reference oscillator then drives a PLL for clock synthesis. The PLL also requires discrete components for the loop filter. These off-chip components, taken together, nearly approach the size of the microcontroller itself.

uses this technique for clock synthesis. In the hybrid approach, only the crystal and a few supporting devices are off-chip, while the remainder of the electronics are integrated onto the processor, including the sustaining amplifier and the frequency translation circuitry. Figure 2.35 shows a photograph of a mocked-up *Motorola* MC68HC812A4 microcontroller on a PC board. The crystal shown here interfaces to an on-chip sustaining amplifier. Together they comprise the reference oscillator. An on-chip PLL frequency translates this reference signal to the target system clock frequency. The PLL also requires discrete components, including off-chip resistors and capacitors for the loop filter [40].

The most amazing observation is that the crystal and discrete components nearly approach the size of the microcontroller itself and the only function provided by these electronics is synthesis of the reference oscillator signal. In contrast, the microcontroller is a complete processing system for data acquisition, analysis, and manipulation. Therefore, although this is the most common clock synthesis approach employed to date, there is a clear need to move toward monolithic integration, as discussed next.

2.4.3 Monolithic

Monolithic integration of the clock synthesis function has already been sufficiently motivated in this dissertation. Equally compelling, though, is the fact that completely merging the clock generation circuitry on-chip is evidently an active goal of commercial microcon-
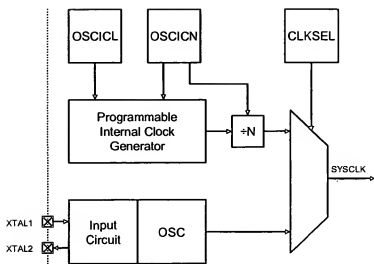
Figure 2.36 Clock generation schematic for the *Cygnal* C8051F06x family. Left of the dotted line is off-chip while right of the dotted line is on-chip. The microcontroller can be clocked from either a crystal-based reference or a completely monolithic ring oscillator. The crystal must be connected off-chip across the ports labeled XTAL1 and XTAL2, along with additional discrete components [41].

troller and microprocessor manufacturers. For example, *Cygnal Integrated Products*, a venture-backed company in Texas, released several families of microcontrollers, some of which include an on-chip clock reference. The C8051F06x family contains a programmable and monolithic free-running clock generation circuit that can be activated in lieu of a hybrid reference oscillator that requires an external crystal, as shown in Figure 2.36 [41]. This monolithic clock circuit is actually nothing more than a programmable on-chip ring oscillator in CMOS. The specification calls for calibration of this reference to compensate for its poor initial frequency accuracy. Referring to Figure 2.36, the register OSCICL must be loaded with the appropriate value to calibrate the ring against a known reference. This is, of course, time consuming and undesirable, but nevertheless it is an illustration of the extent to which microcontroller and microprocessor developers will go in order to eliminate off-chip components.

Additionally it is worth noting that some low-end *Motorola* microcontroller products have been released recently and include free-running relaxation clock oscillators. However, there are clear and substantial shortcomings associated with use of a ring or relaxation oscillator as a clock reference. However, the advantages are compelling and

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include reduced power, component count, size, and cost, along with a wide tuning range and increased reliability. The disadvantages include seriously compromised frequency stability and accuracy. This very topic is the focus of this dissertation, where high stability and accuracy is achieved with reduced power, component count, size, and cost.

2.4.4 Qualitative Comparison

The hybrid PLL/DLL approach to clock synthesis has been popularized due to the fact that several critical system and electrical metrics can be met well with this approach, as shown in Table 2.3. Specifically, with this approach, high-frequency stability and accuracy can be achieved while a compromise is made in the areas of size, cost, tuning range, reliability, and power dissipation. Of course these latter metrics are optimized with current monolithic and free-running implementations, but stability and accuracy are very seriously compromised, which is typically unacceptable. The discrete implementation is becoming less common in modern microelectronic systems, simply due to the fact the there is no benefit over a hybrid implementation. Discrete implementations are typically found only where the microprocessor or microcontroller does not contain the circuitry for the sustaining amplifier and frequency translation circuitry.

Upon examination of Table 2.3, an obvious question arises: what if high frequency accuracy and stability could be achieved with a monolithic approach? The answer, of course, is that this would then become the best option for clock synthesis.

Metric	Discrete (crystal + PLL)	Hybrid (crystal + PLL)	Monolithic (i.e. Ring)
Cost	Expensive	Moderate	Inexpensive
Size	Large	Moderate	Small
Power dissipation	High	Moderate	Low
Tuning range	None (w/o PLL)	None (w/o PLL)	Wide
Reliability	Good	Good	Excellent
Frequency stability	Excellent	Excellent	Poor
Frequency accuracy	Excellent	Excellent	Poor

Table 2.3 A qualitative performance summary of state-of-the-art clock synthesis approaches.

2.5 Conclusions

In this chapter, the concept of clock synthesis has been presented along with several critical metrics that measure the performance of such systems. A theoretical background of oscillators including system analysis, classes, topologies, and models was also presented. The harmonic oscillator was identified as the best choice for stable frequency synthesis. The complementary cross-coupled topology was identified as the best topology for monolithic oscillator development.

The state-of-the-art for clock synthesis was presented as three distinct implementations: discrete, hybrid, and monolithic. Synthesizers can also be classified further as free-running or phase/delay-locked. Currently, there are benefits and shortcomings associated with each approach. However, if a stable and accurate free-running monolithic clock synthesis system could be developed, it has been shown that this would be the clock synthesis approach of choice. The development of such a system is the topic of this dissertation.

CHAPTER III

BOTTOM-UP AND TOP-DOWN APPROACHES TO

STABLE CLOCK SYNTHESIS

In almost all modern synchronous microelectronic systems, a signal from a low-frequency reference oscillator is frequency-multiplied to attain the desired clock signal for the application. Often the multiplicative factor in systems such as these can be on the order of fifty or higher. Though this frequency-multiplication approach is currently ubiquitous in microelectronic design, it has the systemic drawback of significantly degrading the short-term frequency stability. Here, an alternative approach to clock synthesis is proposed which involves the generation of a stable high-frequency clock and division of this signal to lower frequencies for the application. With this top-down approach, the short-term stability is actually enhanced by the same factor by which it is degraded in the clock multiplication method. The subsequent analysis and simulation demonstrate that for a common application, a top-down clock synthesis approach achieves comparable stability performance to bottom-up synthesis, while being substantially simpler to implement and possible to integrate into monolithic form.

3.1 Effects of Frequency Translation on Frequency Stability

Recall that phase and frequency are related by a linear operator and specifically frequency is the time differential of phase, as given by,

$$\omega = \frac{d\phi}{dt} \qquad (3.1)$$

where ω is the radian frequency, ϕ is phase, and t is time. Therefore frequency multiplication will also result in phase multiplication and frequency division will result in phase division. The effect that this observation has on the short-term stability of a periodic signal will be examined next.

3.1.1 Phase Noise

Consider the noisy periodic voltage signal, $v_n(t)$, as a function of time t,

$$v_n(t) = V_1 \cos(\omega_o t + \phi_n(t)) \tag{3.2}$$

where V_1 is the nominal voltage amplitude, ω_o is the fundamental radian frequency, and $\phi_n(t)$ is the phase noise. If this signal is frequency multiplied by an integer N, the output signal is then described by,

$$v_{n,N}(t) = V_1 \cos(N\omega_o t + N\phi_n(t)) \tag{3.3}$$

where phase noise contributed by the multiplication circuitry has been ignored. Clearly the phase noise component of the signal has been increased by N. More importantly, though, by using the narrowband angle modulation approximation, it can be shown that the phase noise power has increased by N^2.

One can rewrite the expression in (3.3) in exponential form,

$$v_{n,N}(t) = Re[V_1 e^{j(N\omega_o t + N\phi_n(t))}] \tag{3.4}$$

and then reduce the expression in (3.4) as follows,

$$v_{n,N}(t) = Re[V_1 e^{jN\omega_o t} e^{N\phi_n(t)}] \tag{3.5}$$

$$= Re[V_1 e^{jN\omega_o t}(\cos N\phi_n(t) + j\sin N\phi_n(t))] \tag{3.6}$$

Assuming $N\phi_n(t)$ is small and using the small angle approximation one can arrive at the following,

$$v_{n,N}(t) \approx Re[V_1 e^{jN\omega_o t}(1 + jN\phi_n(t))] \tag{3.7}$$

$$= Re[V_1(\cos N\omega_o t + j\sin N\omega_o t)(1 + jN\phi_n(t))] \tag{3.8}$$

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$$= V_1 \cos N\omega_o t - V_1 N\phi_n(t) \sin N\omega_o t \tag{3.9}$$

Only the second term in (3.9) is dependent on the phase noise process $\phi_n(t)$. Without frequency multiplication, the expression in (3.9) becomes,

$$v_n(t) = V_1 \cos \omega_o t - V_1 \phi_n(t) \sin \omega_o t \tag{3.10}$$

Clearly the component due to phase noise in (3.9) is increased in amplitude by N, as compared to (3.10), when the frequency is multiplied.

Now consider only this second term in (3.10), which is a stochastic process, and where there is no frequency multiplication. Let the autocorrelation function of this process be given by $R_{v\phi_n}(t_1, t_2)$, which is the portion of $v_n(t)$ that is noise. Then consider the second term in (3.9), which is also a stochastic process, and where the frequency has been multiplied by N. Let the autocorrelation function of this process be given by $R_{v\phi_{n,N}}(t_1, t_2)$, which is the portion of $v_{n,N}(t)$ that is noise. Next find $R_{v\phi_{n,N}}(t_1, t_2)$ in terms of $R_{v\phi_n}(t_1, t_2)$. Using the definition of the autocorrelation function,

$$R_{v\phi_{n,N}}(t_1, t_2) = E[V_1 N\phi_n(t_1)\sin N\omega_o t_1 V_1 N\phi_n(t_2)\sin N\omega_o t_2] \tag{3.11}$$

$$= N^2 E[V_1 \phi_n(t_1)\sin N\omega_o t_1 V_1 \phi_n(t_2)\sin N\omega_o t_2] \tag{3.12}$$

$$= N^2 R_{v\phi_n}(t_1, t_2) \tag{3.13}$$

Assume $R_\phi(t_1, t_2)$ is stationary and thus depends only on the time difference $t_1 - t_2 = \tau$.

$$R_{v\phi_{n,N}}(\tau) = N^2 R_{v\phi_n}(\tau) \tag{3.14}$$

Lastly, recall that the PSD and autocorrelation function of a stochastic process are Fourier transform pairs. Therefore, the PSD for the case without frequency multiplication is given by,

$$S_{v\phi_n}(\omega) = \int_{-\infty}^{\infty} R_{v\phi_n}(\tau) e^{j\omega\tau} d\tau \tag{3.15}$$

and in the case of frequency multiplication, the PSD is given by,

$$S_{v\phi_{n,N}}(\omega) = \int_{-\infty}^{\infty} R_{v\phi_{n,N}}(\tau)e^{j-\omega\tau}d\tau = \int_{-\infty}^{\infty} N^2 R_{v\phi_n}(\tau)e^{-j\omega\tau}d\tau = N^2 S_{v\phi_n}(\omega) \qquad (3.16)$$

where the noise power has clearly increased by N^2, as compared to the case without frequency multiplication.

Returning to the previous discussion, consider a periodic signal, $v_n(t)$, which is divided in frequency by an integer N,

$$v_{n,1/N}(t) = V_o \cos\left(\frac{\omega_o t}{N} + \frac{\phi_n(t)}{N}\right) \qquad (3.17)$$

where the phase noise contribution from the divider circuitry has been ignored. By the same argument just presented, the phase noise is reduced by N and the noise power is reduced by N^2.

Given the results from this discussion, the single sideband phase noise PSD is clearly degraded by N^2 in the case of frequency multiplication and it is improved by N^2 in the case of frequency division. Let the phase noise PSD prior to frequency translation be called $(N_o/P_o)_{f_m}$. After frequency multiplication, let it be called $(N_o/P_o)_{f_m, N}$ and after frequency division, let it be called $(N_o/P_o)_{f_m, 1/N}$. Then,

$$\left(\frac{N_o}{P_o}\right)_{f_m, N} = N^2 \left(\frac{N_o}{P_o}\right)_{f_m} \qquad (3.18)$$

or in units of dBc/Hz,

$$\left(\frac{N_o}{P_o}\right)_{f_m, N} = \left(\frac{N_o}{P_o}\right)_{f_m} + 20\log(N) \qquad (3.19)$$

and

$$\left(\frac{N_o}{P_o}\right)_{f_m, 1/N} = \frac{1}{N^2} \left(\frac{N_o}{P_o}\right)_{f_m} \qquad (3.20)$$

or in units of dBc/Hz,

$$\left(\frac{N_o}{P_o}\right)_{f_m, \, 1/N} = \left(\frac{N_o}{P_o}\right)_{f_m} - 20\log(N) \qquad (3.21)$$

Clearly the degradation or improvement becomes substantial as N becomes large. Recall that in many applications N can be as large as fifty or higher. In a subsequent section, it will be shown how severely this degrades the phase noise and timing jitter.

3.1.2 Period Jitter

Interestingly, frequency division of a periodic signal causes the period jitter to increase. A divider circuit will output only one pulse for N input pulses and thus the variance of the output period is the sum of the variances of the N input periods because of statistical independence of the position of each pulse in time. Since the period jitter is simply the standard deviation of the period, the jitter of a signal divided in frequency by N is given by,

$$J_{1/N} = \sqrt{N}J \qquad (3.22)$$

where J is the period jitter before division. One can also show the same result using the expression relating phase noise to jitter, which has been derived in (2.82). A periodic signal divided in frequency by N will have a phase noise density that is reduced by N^2. Substituting yields,

$$J_{1/N} = \sqrt{\frac{f_m^2}{(f_o/N)^3}\frac{1}{N^2}\left(\frac{N_o}{P_o}\right)_{fm}} = \sqrt{\frac{Nf_m^2}{f_o^3}\left(\frac{N_o}{P_o}\right)_{fm}} = \sqrt{N}J \qquad (3.23)$$

In contrast, multiplication actually reduces the period jitter by the same factor. This may seem, at first, counter intuitive as the phase noise PSD is reduced substantially by division and increased substantially by multiplication. Recall that period jitter is simply a variance. Therefore, it is more illustrative to describe the relative period jitter, J_{ppm}, in parts per million (ppm) as given by,

$$J_{ppm} = \frac{J}{T/10^6} \qquad (3.24)$$

where T is the period. Therefore the relative period jitter for a signal divided in frequency by N is given by,

$$J_{ppm, 1/N} = \frac{J}{\sqrt{N}T/10^6} \tag{3.25}$$

and clearly the relative period jitter is reduced by frequency division. The relative period jitter is increased by the same factor in the case of frequency multiplication. That analysis is identical to the one presented here, but it is not shown because it is trivial.

3.1.3 Allan Variance

The relationship between phase noise and Allan variance has been derived in Chapter II and is presented here again in (3.26),

$$\sigma_y^2(\tau) = \left(\frac{1}{2\pi f_o}\right)^2 \int_0^\infty \left(\frac{N_o}{P_o}\right)_{f_m} \frac{(\sin \pi f \tau)^4}{(\pi f \tau)^2} df \tag{3.26}$$

Using this relationship, consider the effect of frequency multiplication by N and rewrite (3.26) with a fundamental frequency of Nf_o and a phase noise PSD as given in (3.18). Call the new Allan variance for the frequency translated signal $\sigma_{y,N}^2(\tau)$.

$$\sigma_{y,N}^2(\tau) = \left(\frac{1}{2\pi N f_o}\right)^2 \int_0^\infty N^2 \left(\frac{N_o}{P_o}\right)_{f_m} \frac{(\sin \pi f \tau)^4}{(\pi f \tau)^2} df \tag{3.27}$$

$$= \left(\frac{1}{2\pi f_o}\right)^2 \int_0^\infty \left(\frac{N_o}{P_o}\right)_{f_m} \frac{(\sin \pi f \tau)^4}{(\pi f \tau)^2} df \tag{3.28}$$

$$= \sigma_y^2(\tau) \tag{3.29}$$

The Allan variance does not change with frequency translation. This may seem surprising because it is clear that frequency translation affects the phase noise and the period jitter very significantly. Consider (3.26) more closely and ignore the shaping caused by the trigonometric term. Clearly Allan variance is related to the phase noise PSD by integration

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Variable/Metric	Reference oscillator	Bottom-up synthesis	Top-down synthesis
Output frequency (Hz)	f_{ref}	Nf_{ref}	f_{ref}/N
Phase noise PSD (dBc/Hz)	$\left(\dfrac{N_o}{P_o}\right)_{fm}$	$\left(\dfrac{N_o}{P_o}\right)_{fm} + 20\log N$	$\left(\dfrac{N_o}{P_o}\right)_{fm} - 20\log N$
Phase noise PSD degradation/improvement	—	$20\log N$	$-20\log N$
Period jitter (s)	J	$J/\sqrt{N}$	$\sqrt{N}J$
Period jitter degradation/improvement	—	$1/\sqrt{N}$	$\sqrt{N}$
Relative period jitter (ppm)	J_{ppm}	$J_{ppm}\sqrt{N}$	$J_{ppm}/\sqrt{N}$
Relative period jitter degradation/improvement	—	$\sqrt{N}$	$1/\sqrt{N}$
Allan variance	$\sigma_y(\tau)$	$\sigma_y(\tau)$	$\sigma_y(\tau)$

Table 3.1 Summary of frequency stability expressions for bottom-up and top-down synthesis.

of the density normalized by the square of the fundamental frequency. Thus, the degradation in phase noise is cancelled by frequency normalization. This should be obvious because frequency translation by N also changes the variance by N and thus there is no net change in variance.

A summary of all derived short-term frequency stability relationships is presented in Table 3.2. These results will be used in the sections that follow.

3.2 The Relationship with Q

The LTI expression for the phase noise PSD of a generalized resonant oscillator can be described by the classic Leeson model presented in Chapter II,

$$\left(\frac{N_o}{P_o}\right)_{f_m} = \frac{1}{8Q^2}\frac{FkT}{C}\left(\frac{f_o}{f_m}\right)^2 \tag{3.30}$$

where F is the circuit noise factor, k is Boltzmann's constant, T is temperature, C is the oscillator output power, Q is the resonant device quality factor, f_o is the oscillator funda-

mental frequency, and f_m is the frequency offset from the fundamental. Note that Q is quadratically related to the phase noise PSD in an inverse relationship as compared to the frequency multiplication factor N.

One could consider that frequency multiplication and division effectively and respectively degrade and enhance the quality factor of the reference oscillator. Therefore it is possible that a very high-Q reference oscillator, with $Q = Q_m$, that is multiplied in frequency by the factor N_m and a very low-Q reference oscillator, with $Q = Q_d$, that is divided in frequency by the factor N_d may have the same short-term stability performance at the application frequency. Given that the phase noise PSD is quadratic in both Q and frequency translation, N, one can determine the rough estimate that if,

$$N_d N_m \geq \frac{Q_m}{Q_d} \tag{3.31}$$

then the short-term stability of the divided signal will be comparable to that of the multiplied signal. Of course, this relationship ignores the noise contribution of additional circuit components and assumes that the noise factor and oscillator power are the same for both references, which may not be the case. Nevertheless, the expression is useful in the sense that it captures the notion of stability degradation due to frequency translation.

3.3 Top-Down and Bottom-up Frequency Synthesis

3.3.1 A Bottom-Up Approach

Typically bottom-up synthesis is achieved with the use of a PLL or DLL. Figure 3.1 illustrates the components of a simple PLL. The reference oscillator is compared against a frequency divided image of the VCO output. The phase-frequency detector (PFD) drives a charge pump (CP) and a low pass filter (LPF) that sets the control voltage, v_{ctrl}, for the VCO. The PLL effectively multiplies the reference oscillator frequency, f_{ref}, to Nf_{ref}. Systems such as these are fairly simple to develop and are capable of synthesizing a wide variety of frequencies. When an additional divider is placed in front of the reference oscillator, fractional multiplication can be achieved. Several other topologies and variations of
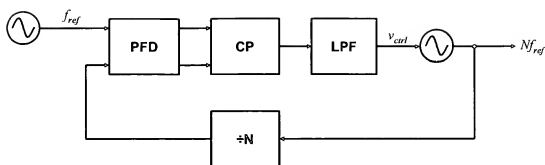
Figure 3.1   A typical PLL-based bottom-up clock synthesis system. A frequency divided image of the output is compared against the reference oscillator by the PFD. The CP and LPF filter the signal from the PFD and generate the control voltage for the VCO.

bottom-up synthesis exist, but the simplest approach is most appropriate for this analysis because it can be extended easily to any other topology.

Other drawbacks associated with PLL and DLL systems include the accumulated frequency instability and the number of components required for system implementation, which ultimately translates into power dissipation and silicon area. Moreover, the PLL has a long lock time for large frequency changes, which is undesirable in many applications.

3.3.2 A Direct Synthesis Approach

It is worth noting that one could simply directly synthesize the desired clock frequency from a monolithic harmonic oscillator, such as an inductor-capacitor, or LC, oscillator. However, many embedded processors operate at relatively low clock frequencies as compared to the maximum frequency that can be achieved in a given manufacturing process technology. For example, the ubiquitous *Intel* SA-1110 microprocessor operates at up to approximately 200MHz [42], even though the process for this device supports frequencies well over 1GHz. In order to develop an LC clock synthesizer at 200MHz, an inductance of approximately 25nH and a capacitance of approximately 25pF would be required. A 4.5 turn inductor of this size would be over 500μm in diameter. Similarly, even with a high density capacitor option where the capacitance per unit area is on the order of 1fF/μm^2, the area for the capacitor would be 25,000μm^2. Without the high-density capacitor option, this area requirement can increase by a factor of 10 or more. Lastly, the short stability of this oscil-

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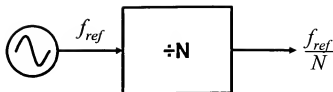
Figure 3.2 The proposed simple top-down clock synthesis system. Only a reference oscillator and divider circuit are required.

lator would be determined entirely by the performance of the oscillator at 200MHz and any enhancement due to frequency translation would not be realized.

3.3.3 A Top-Down Approach

An alternative approach to clock generation would be to directly synthesize the desired frequencies by division of a stable high-frequency reference. The system, as shown in Figure 3.2, would be significantly simpler than the bottom-up approach and would permit instantaneous frequency changes. Of course, additional electronics would be required for fractional-N synthesis, similar to the bottom-up technique. This architecture also permits integration of passive devices that are reasonably sized.

The most formidable challenge associated with this approach is that the reference oscillator must be highly stable and accurate. The development of such a reference, which ultimately enables monolithic clock generation that requires no external components, is the focus of this dissertation.

3.4 Application, Design, and Simulation

A common application for clock synthesis has been selected as a test bench for analysis. The *Compaq* iPAQ 3600 uses the *Intel* SA-1110 microprocessor. The processor runs up to approximately 200MHz from a 3.6864MHz crystal reference oscillator. An on-chip PLL is utilized to frequency multiply the reference signal [42].

A simulation bench for each clock synthesis approach has been developed for this application. The reference oscillator for both the bottom-up and top-down approach have been designed using the RF noise models, including device thermal and flicker noise, for

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the 0.18μm mixed-mode process available from *Taiwan Semiconductor Manufacturing Company*. Although both jitter and phase noise can be simulated for these reference oscillators, it is typically significantly easier to simulate phase noise because it is performed in the frequency-domain. Time-domain simulations and subsequent statistical analysis require significant data space and simulation time [43]. The tool used for these simulations was *Cadence SpectreRF*.

The top-down simulation bench includes the developed reference oscillator and device-level D flip-flops for frequency division. The entire system can be simulated using *SpectreRF*.

The bottom-up system is difficult to simulate within a reasonable time and with a manageable amount of data. This is because the phase noise analysis in *SpectreRF* requires periodic steady-state convergence. This convergence takes a significant amount of time including reference oscillator start-up, loop acquisition, and lock. Moreover, the time-domain step interval must be very small because the PLL output frequency is 200MHz. The Q-factor for the reference oscillator crystal is 10,000 and thus the start-up time is on the order of several hundred milliseconds, further confounding the problem. The PLL lock time is also several milliseconds. Thus, a different approach is required to simulate the bottom-up system. Here a phase-domain hardware description language (HDL) model was utilized as shown in [26]. The data from the phase noise simulation of the device-level reference oscillator are modeled in HDL, specifically *Verilog-A*. This phase-domain technique models only the phase noise and thus no high-frequency voltage-domain signals are present, which simplifies the simulation substantially. The same technique is employed for the voltage controlled oscillator (VCO) contained within the PLL. The remainder of the components are also modeled in the phase domain, with the exception of the loop filter and phase detector. The complete system is constructed from these modules, as will be described.

3.4.1 Bottom-Up Synthesis Reference Oscillator

In the bottom-up approach, the clock signal is generated from a crystal reference oscillator as shown in Figure 3.3. The crystal has been modeled as a lumped series *RLC* circuit with
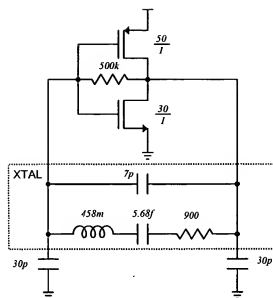
Figure 3.3   3.125MHz Pierce crystal reference oscillator with the crystal modeled as lumped *RLC*.

parasitics, per a common manufacturers specification. The quality factor of the device is 10,000 and the series resonant frequency is 3.125MHz. This particular resonant frequency deviates slightly from the *Intel* specification, but does not create a loss of generality in the analysis. It simply allows for integer frequency relationships.

A Pierce oscillator configuration was developed around the crystal because it is a low phase noise topology and a common implementation for clock generation, as described in Chapter II. The reference oscillator drives the phase detector and the remainder of the PLL, as shown in Figure 3.1.

The Pierce reference oscillator was simulated with *SpectreRF* at the device level in order to accurately determine the phase noise performance of the circuit. These results were then used to develop the *Verilog-A* phase-domain model, which is described in detail later.

3.4.2 Bottom-Up Synthesis VCO

A simple current-starved voltage-controlled ring oscillator was designed for the bottom-up synthesis system, shown in Figure 3.4. The VCO has 11 inverter stages with a nominal delay of 227ps per gate with a nominal oscillation frequency of 200MHz. The bias voltage on the gates of the PMOS devices controls the amount of current that flows into each gate
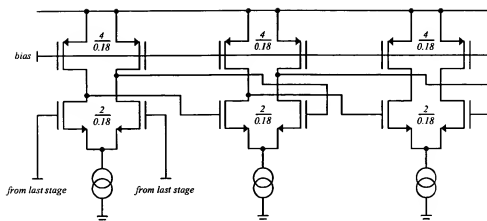
Figure 3.4   First 3 stages of 11-stage current-starved voltage-controlled ring oscillator. The bias on the gates of the PMOS devices controls the current in each stage, thus modulating the oscillation frequency.

and modulates the oscillation frequency. This circuit was simulated at the device level and the phase noise performance was determined. The data were used to develop the phase-domain *Verilog-A* model for the VCO, which is also presented later.

3.4.3 Phase-Domain HDL Model of the Bottom-Up Synthesis Approach

As described previously, using a phase-domain approach significantly reduces the complexity of simulating a complete PLL. Referring back to Figure 3.1, all of the components of this bottom-up synthesis system have been modeled in the phase-domain using *Verilog-A,* except for the loop filter and the phase detector. These two modules were not designed entirely in the phase domain for the purposes of development simplicity and simple electrical analogy.

A voltage-domain low pass filter was designed using an ideal op-amp, as shown in Figure 3.5, for the loop filter. The 3dB bandwidth of the filter is set by the *RC* component values within the circuit and is thus approximately 230kHz. A mixed-domain model was used for the phase detector. Specifically, phase is detected at the input of the module and current is driven out to the voltage-domain loop filter.

The source code for all of the components, except the loop filter, is listed in the tables that follow. The function *flicker_noise(pwr, α, label)*, used in the listings below,

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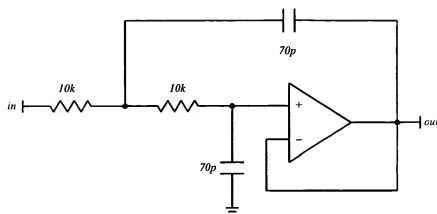
Figure 3.5 Schematic of the 2nd-order Butterworth low-pass loop filter. The bandwidth is set by the RC components and is 230kHz.

takes the arguments *pwr*, α, and *label* where α is the exponent of frequency in the form of $1/f^{\alpha}$, *pwr* is the noise power at 1Hz, and *label* is simply an identifier for the noise component. This function is particularly useful because noise of any exponent in frequency can be modeled. However, only flicker of frequency $(1/f^3)$ and white of frequency $(1/f^2)$ phase noise have been modeled since these regions comprise the majority of the phase noise PSD for oscillators, as described in Chapter II. The function *flicker_noise* was utilized to model the results from device-level simulation as closely as possible. The variables n and f_c are also used in some instances of the function in order to provide intuitive and parameterized model where n is the power at 1Hz and f_c is the corner frequency, or the break point where the phase noise density slope changes from $1/f^3$ to $1/f^2$.

The function *white_noise(pwr, label)*, simply takes arguments *pwr* and *label* where *pwr* is the white noise power and *label* is again some unique identifier for the source. *Theta(out)* sets the output phase for each module, which is driven by these noise components. Lastly, the function *idt(x)* returns the time integral of x from 0 to t and M_PI is π. A complete listing for all components can be found on the next two pages.

3.4.4 Top-Down Synthesis Reference Oscillator

The top-down design included a highly-stable 3.2GHz CMOS-*LC* oscillator, shown in Figure 3.6, and a series of 4 D flip-flops for frequency division. The loaded quality factor

Verilog-A **phase-domain reference oscillator model**

```
'include "constants.h"
'include "discipline.h"


discipline phase
    potential Angle;
enddiscipline


module oscillator(out);
output out;
phase out;


parameter real n=340e-11 from [0:inf);    // phase noise at 1Hz (rad^2/Hz)
parameter real fc=60 from [0:inf);         // flicker noise corner frequency (Hz)


analog begin
    Theta(out)<+flicker_noise(0.7e-12,0.9,"wpn") + flicker_noise(n*fc,3,"fpn")+white_noise(10e-16,"epn");
end


endmodule
```

Table 3.2 *Verilog-A* listing of the phase-domain reference oscillator module.

Verilog-A **mixed-domain phase detector model**

```
'include "constants.h"
'include "discipline.h"


discipline phase
    potential Angle;
enddiscipline


module phasedetector(pin,nin,out);
input pin,nin;output out;
phase pin,nin;
electrical out;


parameter real gain=1 from (0:inf);     // transfer gain (A/cycle)


analog begin
    I(out)<+gain*Theta(pin,nin)/(2*M_PI);
end


endmodule
```

Table 3.3 *Verilog-A* listing of the mixed-domain phase detector module.

Verilog-A phase-domain divider model

```
'include "constants.h"
'include "discipline.h"


discipline phase
     potential Angle;
enddiscipline


module divider(in,out);
input in;output out;
phase in,out;
parameter real ratio=64 from (0:inf);        // divide ratio


analog begin
     Theta(out)<+Theta(in)/ratio;
end


endmodule
```

Table 3.4 *Verilog-A* listing of the phase-domain divider module.

Verilog-A phase-domain VCO model

```
'include "constants.h"
'include "discipline.h"


discipline phase
     potential Angle;
enddiscipline


module vco(in,out);
input in;output out;
voltage in;
phase out;
parameter real gain=10e6 from (0:inf);         // transfer gain, Kvco (Hz/V)
parameter real fc=1e3 from [0:inf);            // flicker noise corner frequency (Hz)
parameter real n=1000e-1 from [0:inf);         // phase noise at 1Hz (rad^2/Hz)


analog begin
    Theta(out)<+2*`M_PI*gain*idt(V(in),0);
    Theta(out)<+flicker_noise(n,2,"wpn")+flicker_noise(n*fc,3,"fpn")+white_noise(1e-15,"epn");
end


endmodule
```

Table 3.5 *Verilog-A* listing of the phase-domain VCO module.
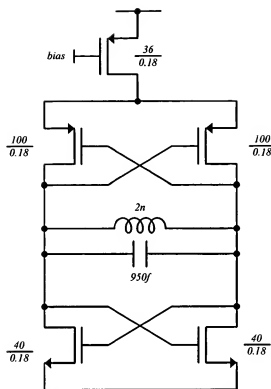
Figure 3.6   3.2GHz complementary cross-coupled negative-g_m CMOS-LC top-down reference oscillator.

of the LC tank was estimated to be approximately 10. The sustaining amplifier is a complementary cross-coupled topology, which generates a negative resistance to cancel the loss in the tank. The complete top-down system was simulated at the device level in *SpectreRF*. No HDL models were used for simulation of this system. Consequently, the noise of the divider flip-flops is included.

3.5 Results

Table 3.6 summarizes the results from the simulation and analysis. The frequency division factor in the top-down approach was 16 and thus the theoretical phase noise improvement was 24.1dB. The simulated improvement was 23.8dB, indicating that the divider circuit contributed only slightly to the overall phase noise. In contrast, the frequency multiplication factor in the bottom-up approach was 64, which corresponds to a theoretical phase

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Performance metric	Bottom-up synthesis	Top-down synthesis
Application frequency, f_o (MHz)	200	200
Reference oscillator frequency, f_{ref} (MHz)	3.125	3,200
Multiplication/division factor, N	×64	÷16
Reference oscillator quality factor, Q	10,000	10
Reference oscillator phase noise PSD, $(N_o/P_o)_{fm}$ (dBc/Hz)	-140.8 @ 10kHz offset	-83.0 @ 10kHz offset
Calculated period jitter at reference from $(N_o/P_o)_{fm}$ @ 10kHz offset, J (fs)	165	3.9
Calculated relative period jitter at reference, J_{ppm} (ppm)	0.51	2.8
Synthesizer output phase noise PSD, $(N_o/P_o)_{fm}$ (dBc/Hz)	**-104.6 @ 10kHz offset**	**-106.8 @ 10kHz offset**
Calculated period jitter at output from $(N_o/P_o)_{fm}$ @ 10kHz offset, J (fs)	**21**	**16**
Calculated relative period jitter at output, J_{ppm} (ppm)	**4.2**	**3.3**
Phase noise PSD accumulation/reduction factor, (dB)	+36.2	-23.8
Period jitter accumulation/reduction factor	0.12	4.1
Relative period jitter accumulation/reduction factor	8.2	0.24

Table 3.6 Performance metric comparison between bottom-up and top-down frequency synthesis approaches. The performance at the target frequency is nearly identical, as shown in bold.

noise degradation factor of 36.1dB. The simulated degradation was 36.2dB. Phase noise PSD plots for each approach are shown in Figure 3.7 and Figure 3.8.

Phase noise induced jitter for the bottom-up system can be determined using (2.78), but it is simpler to bound the phase noise PSD and select an appropriate position at which the jitter can be estimated from the phase noise, using (2.82). Here, the phase noise is bounded on the low end by extrapolation of the phase noise where the slope is 20dB/dec. The upper bound is set by a line with slope 20dB/dec that intersects the PLL loop bandwidth at 230kHz. Using these bounds, jitter for the bottom-up system was determined at a 10kHz offset, which is within the bound. Jitter was estimated for the top-down system using
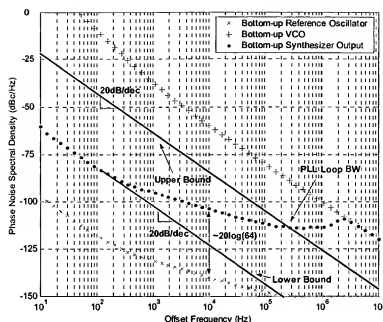
Figure 3.7 Bottom-up reference oscillator and synthesized clock phase noise PSD. The close-to-carrier phase noise PSD was degraded by 36.2dB due to frequency multiplication. The phase noise can be bounded to estimate phase noise induced jitter. The conversion was made at a 10kHz offset, which is within the bound.
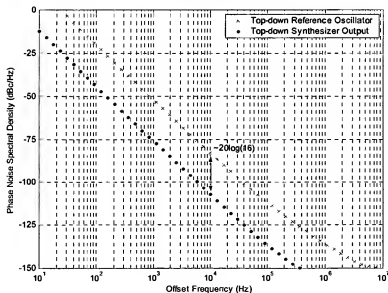
Figure 3.8 Top-down reference oscillator and synthesized clock phase noise PSD. The phase noise PSD was improved by 23.8dB by frequency division.

the same frequency offset. All results are shown in Table 3.6. The most interesting observation is that the top-down approach realizes a frequency stability that is comparable to the

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bottom up approach. The LC oscillator used in the previous approach contained a tank with a quality factor of only 10, while the quality factor of the crystal reference was 10,000. As described previously, the reference quality factor and phase noise degradation factor from frequency multiplication are quadratically and inversely related. The systemic accumulation error introduced in the PLL approach drastically reduces the high-performance delivered by the crystal-based reference. A similar result to the approximation made here can be confirmed by evaluating (2.78). It is also worth considering that the bottom-up synthesis system contains function blocks that introduce synchronous jitter, which was not considered here. Thus, performance of the top-down synthesis system is likely not just comparable, but rather superior to that of the bottom-up system.

Lastly, consider the expression given in (3.31), presented here again

$$N_d N_m \geq \frac{Q_m}{Q_d} \tag{3.32}$$

For this particular design, $N_d = 16$, $N_m = 64$, $Q_m = 10,000$, and $Q_d = 10$. Substituting into (3.32) and evaluating gives, $1024 > 1000$. As predicted, if this condition holds, the phase noise and jitter performance will be better in the case of top-down synthesis than in bottom-up synthesis, as has been confirmed through simulation in this example.

3.6 Conclusions

The relationships describing the effects of frequency multiplication and division on short term clock stability have been analyzed and presented. Using a common application as a test bench, the presented relationships were verified. The proposed top-down approach to clock synthesis has been shown to be a simple free-running alternative to the common phase-locked bottom-up approach, while offering comparable stability. Moreover, the top-down approach facilitates monolithic integration. However, challenges still reside in achieving other metrics such as accuracy and temperature stability. Nevertheless, it has been shown that it is possible to employ top-down frequency synthesis with a monolithic harmonic oscillator and achieve comparable short-term stability performance to a crystal

for a very common processor application, namely the *Intel SA*-1110. This new approach to clock synthesis will be described in detail in subsequent chapters.

CHAPTER IV

STATE-OF-THE-ART HARMONIC MONOLITHIC

OSCILLATORS

The vast majority of active research in the area of monolithic frequency synthesis has been focussed on RF applications. In particular, this research has targeted enhancement of the short-term stability of the VCO that would be contained within a PLL. Success in this endeavor ultimately provides better communication performance in RF systems and reduced bit error rate (BER). The BER in an RF system is directly related to the VCO phase noise as well as the blocking signal specification as is described in Chapter II. Other related and substantial research also exists in the area of PLLs, DLLs, and clock distribution. However, none of this latter research has been pursued in an effort to displace the crystal reference or to achieve monolithic clock generation. Therefore this research will not be discussed here and only attempts to achieve high-performance monolithic frequency synthesis will be addressed.

This chapter begins with a brief discussion of critical metrics for references and continues with an overview of recently presented reference technologies for monolithic harmonic oscillators. Qualitative and quantitative comparisons between existing approaches will be drawn. It will be shown that micromachining presents some of the most compelling opportunities. The chapter continues with a survey of recently published results in the area of monolithic harmonic frequency synthesis. It will be shown that the performance of both the reference device and its use in an oscillator are critical considerations. The chapter closes with a summary of the reference technology that has been identified for this work. The details of this approach and its implementation are covered thoroughly in the next chapter.

4.1 Critical Metrics

Several metrics are worth consideration when studying reference technologies These include quality-factor, size, accuracy, process complexity, linearity, and bias conditions. Not all of these metrics apply equally to all references. For example, a passive inductor performs essentially the same over a wide range of bias conditions. In contrast, a MOS varactor presents several operating regions which may or may not be appropriate depending on the application. Another example includes high-Q micromechanical resonators, the majority of which require a vacuum package to operate and are consequently difficult to integrate with CMOS. In terms of Q-factor, these devices are an excellent choice. In terms of integration, these devices present very serious challenges. In the sections that follow, qualitative analyses such as these are presented for each potential reference technology.

4.2 Monolithic Harmonic Reference Technologies

A breadth of harmonic reference technologies has been presented in an effort to improve the accuracy, stability, and tuning range of monolithic harmonic oscillators. These approaches include enhancement and development of several types of harmonic references and span concepts from alternative techniques for the realization of an inductor to microscopic mechanically resonant devices. The most promising and interesting approaches that have been presented to date are discussed here and are divided into two distinct sections: mechanically resonant and electrically resonant references.

4.2.1 Mechanically Resonant References

Mechanical resonators are devices that physically vibrate, or resonate, at a distinct frequency when excited by an external force that corresponds to the natural frequency of the device. Typically, mechanical resonators exhibit very high frequency selectivity and thus very high Q. The first attempt at building a microscopic mechanically resonant device in CMOS technology was demonstrated in [44] and called "the resonant gate transistor." An illustration of the device is pictured in Figure 4.1. Since this early work, a tremendous amount of research has been pursued to develop a mechanical reference technology that could be realized in CMOS. This recent work is discussed in the following sections.
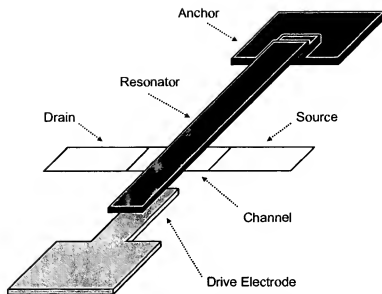
Figure 4.1 Illustration of the resonant gate transistor. The drive electrode excites the resonator, which serves as the gate of the MOS transistor. Displacement of the resonator modulates the channel current, which can be detected and amplified.

4.2.1.1 Electrostatic and Capacitively Coupled Resonators

Electrostatic and capacitively coupled resonators are similar to tuning forks. Here again, the electrical-mechanical analogy presented in Chapter II is useful. Recall that in this analogy, force and voltage are analogous pairs. Using this analogy, consider the tuning fork again. This device is used by striking it with a contact force. The fork then resonates at a distinct frequency, the amplitude of which eventually decays over time. Electrostatic resonators operate upon the same principle. However, the applied force is a voltage, which creates mechanical deflection from capacitive transduction.

One of the simplest electrostatic resonators is a beam clamped at both ends with an electrode underneath, as illustrated in Figure 4.2, and commonly referred to as a clamped-clamped beam resonator [9]. The device is operated by first applying a DC voltage across the beam-electrode gap. Then an AC excitation voltage, v_i, is applied to the electrode and when its frequency matches the natural frequency of the device, the beam will resonate. An electromechanical simulation of this deflection is shown in Figure 4.3. In this simulation, the boundary conditions are set such that the ends of the beam are fixed. Finally, a fabri-

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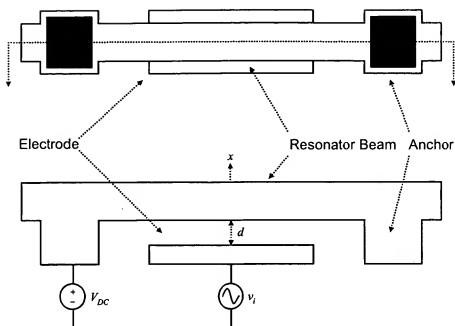
Figure 4.2   Top view and cross-section of a clamped-clamped beam micromechanical resonator. When the frequency of the excitation voltage, v_i, matches the natural frequency of the device, the beam will resonate.

cated surface micromachined 10MHz polysilicon clamped-clamped beam device is shown in Figure 4.4 where the resonator geometry is indicated. This device can be utilized as a reference for frequency synthesis when placed in a loop with a sustaining amplifier. The deflection of the beam creates a change in the capacitance between the beam and the elec-
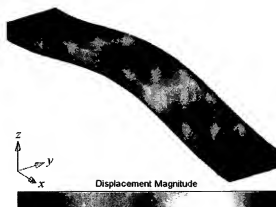
Figure 4.3   Results of a finite element simulation of a clamped-clamped beam microresonator indicating the relative displacement due to an applied voltage. The simulation boundary conditions are set such that the ends of the device are fixed.
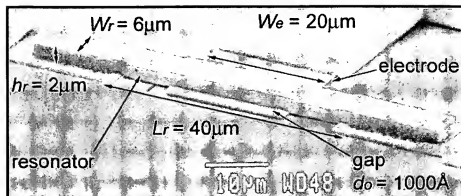
Figure 4.4 Electron micrograph of a fabricated surface micromachined 10MHz clamped-clamped beam resonator in polysilicon.

trode, which then induces a displacement current at the mechanical resonant frequency. This displacement current can be detected, amplified, and sustained.

The resonant frequency of this device can be determined approximately by solving the differential equation for harmonic motion. The solution is,

$$\omega_o = \sqrt{\frac{k}{m}} \tag{4.1}$$

where m is the mass of the beam, k is the stiffness, and ω_o is the fundamental radian frequency. A significantly more advanced analytical approach will be described in Chapter VII. For now, it suffices to identify the fact that the frequency can be scaled by increasing the stiffness of the beam material or by reducing the mass, which naturally translates into reducing the geometry. An additional and less obvious technique for scaling the frequency is to excite the beam in a higher order mode shape. The mode shape shown in Figure 4.3 is the fundamental mode. Higher order modes can be excited with a variety of techniques as shown in [45] and [46].

Two very significant characteristics associated with this type of device are the non-linear transduction and the large motional resistance [9]. The capacitive variation of the device is clearly nonlinear and thus this nonlinearity can result in a variety of undesirable phenomena including frequency pulling and distortion of the resonator transfer function, commonly called duffing [9]. The large motional resistance is an equally undesirable char-

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acteristic of this device. Recall the negative resistance model for an arbitrary oscillator presented in Chapter II. The sustaining amplifier must overcome this resistance. Of course, although the Q-factor of these devices is high, the large motional resistance must still be overcome, which is quite difficult. It is also difficult to use these devices in general RF applications, such as filters, where the typical system impedance is 50Ω.

Several variations of the basic clamped-clamped beam topology have been presented and include comb-drive [47], free-free beam [48], and disk resonators [49]. These devices operate on the same principle of capacitive transduction with differences primarily associated with frequency scaling and linearization of the transduction mechanism. For example, the comb-drive resonator is a linear transducer, but can be fabricated only at kHz frequencies. Free-free beam resonators have been demonstrated at 100MHz and higher, but still suffer from nonlinear transduction identical to the clamped-clamped beam resonator.

Preliminary research pertaining to this dissertation involved the fabrication and test of clamped-clamped beam microresonators, including the polysilicon device shown in Figure 4.4. Results from test are shown in Figure 4.5 and a Q-factor of nearly 1,500 was achieved. These measurements were taken under high vacuum, where the estimated pressure was 20mTorr. The high vacuum is required to prevent mass-loading from environmental contamination, which can modulate the resonant frequency of the device because its mass is so small. The vacuum is also required because the viscosity of air becomes substantial relative to the small geometry of these devices. The damping caused by air significantly
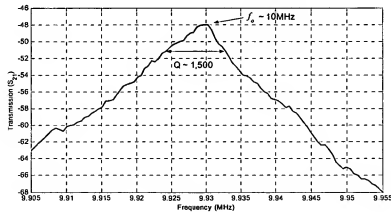
Figure 4.5 S_{21} plot of 10MHz surface micromachined polysilicon resonator acquired with an HP4195 vector network analyzer. The measured quality factor is approximately 1,500.

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degrades the performance of the device and typically the deflection cannot be sensed at a reasonable AC signal amplitude.

The device presented in Figure 4.4 and the majority of devices previously demonstrated and summarized in [50] have been fabricated in polysilicon. Thus, some type of custom modification to a standard CMOS process is required. Several approaches have been adopted to integrate polysilicon MEMS with CMOS. These include a preprocessing MEMS-first approach, such as *Sandia's* iMEMS process [51]; a mixed MEMS and circuits technique, such as *Analog Devices'* iMEMS process [52]; and a post-processing, MEMS-last approach, such as *UC-Berkeley's* MICS process [9]. Impressive results have been reported from each. Nevertheless, the likelihood that these processes would become standardized remains quite small due to the cost, complexity, and specialized nature of each process. For example, *Berkeley's* MICS process is almost exclusively for surface micromachined resonators while *Analog Devices'* iMEMS process has been developed primarily for bulk micromachined inertial sensors.

Mechanical microresonator research is an interesting and exciting field of study. However, the CMOS integration processes reported to date are complex and expensive. The requirement of vacuum packaging further complicates integration. Some devices have been reported recently with high Q-factors in air [53], but still in a polysilicon process. Likely, microresonators will be utilized in applications where multiple reference devices are required and thus several crystals can be replaced by one vacuum packaged device containing several microresonators. However, the likelihood of low-cost CMOS integration, at this point, is quite low. Also, very recent work [54] indicates that the nonlinear capacitive transduction associated with these devices severely degrades the phase noise performance when references such as these are utilized in a frequency synthesis application. This problem, more than any other, will ultimately determine the utility of this reference technology.

4.2.1.2 Piezoelectric Resonators

Piezoelectric resonators operate on the principle of piezoelectric effect. When an electric field is applied across a piezoelectric material, the device deforms mechanically. This deformation induces a current which can be amplified and sustained. The ubiquitous dis-
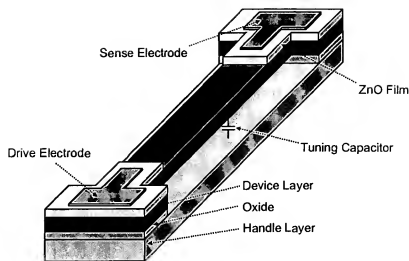
Figure 4.6 Tunable ZnO piezoelectric resonator fabricated from a silicon-on-insulator (SOI) substrate. The beam is suspended by etching the SOI BOX and can be deflected and sensed by piezoelectric effect. The resonant frequency can also be tuned by applying a DC voltage between the handle and the beam, which modifies the beam stiffness [55].

crete quartz crystal is a piezoelectric device. As such, it comes as no surprise that attempts to realize an equivalent microscale device on a Si substrate have been well underway.

In [55] a piezoelectrically actuated mechanical resonator was reported using a silicon-on-insulator (SOI) substrate. A diagram of the device is presented in Figure 4.6. The device is basically a clamped-clamped beam microresonator with the exception that the piezoelectric material, ZnO in this case, is placed over the anchors and part of the beam. An electrical signal that is applied to the drive electrode will cause the piezoelectric material to deform and thus deflect the beam. This deflection can be detected by piezoelectric transduction at the sense electrode. The beam is constructed from the device layer of the SOI wafer. It is released by etching the buried oxide (BOX). ZnO is sputtered and patterned and the electrodes are defined with an aluminum lift-off process. The device can also be tuned by applying a voltage between the handle and the beam. Doing so introduces an electrostatic force, causing the beam to bend and stiffen, thus modulating the resonant frequency. The reported design achieves a quality factor on the order of 5,000 at a resonant frequency of 0.721MHz while under a vacuum pressure of 50mTorr.

This reported design posses several interesting benefits over the capacitively coupled clamped-clamped beam structure described previously. First, the device is simpler to

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fabricate. Second, the ZnO film increases the electromechanical coupling and thus reduces the motional resistance. Lastly, the resonator is fabricated in single-crystal silicon, as opposed to polycrystalline silicon, and thus the associated Q-factor is much higher.

The drawbacks associated with this work again include the non-standard fabrication process and the vacuum requirement. Also, the starting substrate must be SOI, which at the time of this writing, is an expensive substrate due to low-volume production. However, even if an SOI substrate were to become the standard for CMOS, which is not unlikely in the near term, the device reported here is fabricated with a thick device layer that is 4µm. The handle layer of a typical SOI-CMOS substrate is approximately 3000Å and thus another significant hurdle must be overcome in order to integrated these devices with CMOS. Most likely, the best application for these devices is the same as for the capacitively transduced devices.

Another class of piezoelectric device has been reported in [56]. These are thin film bulk acoustic resonators or FBARs. A diagram illustrating this device is shown in Figure 4.7. Here a thin piezoelectric film, typically ZnO, is deposited on a substrate. However, a reflector material is first placed underneath this film in order to isolate the acoustic fields
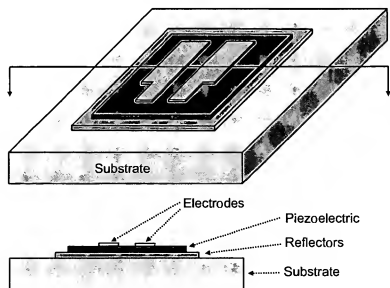
Figure 4.7   Illustration of an FBAR device on a Si substrate. Reflectors isolate the acoustic fields generated by the resonator. The electrodes drive and sense the piezoelectric material.

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that are generated by the resonator from the substrate. Then drive and sense electrodes are placed over the film.

These devices have been reported with quite impressive results and have recently been deployed in commercial RF electronics. The Q-factors achieved are on the order of several thousand and no vacuum packaging is required. Additionally, the motional resistance is very low, making these devices well-suited to RF applications. However, these devices are still fabricated with a process technology that is difficult to integrate with CMOS electronics. Moreover, the geometric dimensions of FBAR devices is substantially larger than the microresonators described previously. Typical FBAR dimensions are on the order of millimeters while typical microresonator dimensions are on the order of microns. Thus, integration with CMOS is unlikely, but these devices will likely continue to be a small and low-cost alternative to quartz crystals.

Microscale piezoelectric resonators are also an exciting field of research, but will likely remain as a discrete solution that can displace quartz crystals, particularly in applications where multiple crystal references and filters are required. Despite the promising and exciting work reported to date, these technologies are not yet an appropriate reference for clock synthesis in CMOS.

4.2.2 Electrically Resonant References

Given the challenges associated with the mechanical references described, an electrically resonant reference has been identified as the most appropriate device for this work. An electrically resonant harmonic device is a coupled inductor and capacitor or varactor. These devices can be developed easily in most modern CMOS process technologies. However, the drawback associated with electrical references is low Q-factor. Loss due to several mechanisms in both the inductor and varactor structure presents a significant challenge. Several promising and successful approaches have been developed to overcome this challenge and are presented next.

4.2.2.1 Inductors

An inductor serves as the magnetic storage element in an electrically resonant LC-tank, as described in Chapter II. Although an LC-tank is fairly simple to integrate with CMOS, significant drawbacks associated with it are its size and the low quality factor due to a variety of loss mechanisms, many of which are associated with the substrate. The inductor is typically the most lossy element in an LC-tank and thus optimization of its performance is a popular research topic.

Consider the simple hollow-core square spiral inductor shown in Figure 4.8. The inductance of a structure like this is often calculated using Green's formulation with the aid of a simulation tool, but with the use of a simple model, the inductance of this structure can be estimated by the following relationship [3],

$$L \approx \frac{37.5\mu_o n^2 a^2}{22r - 14a} \tag{4.2}$$

where a is the mean radius of the spiral, n is the number of turns, μ_o is the permeability of free space, and r is the outer radius of the spiral. Interestingly, as a is decreases (which
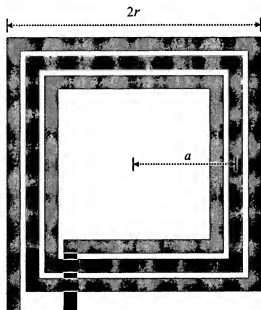
Figure 4.8 A hollow-core square spiral inductor. An estimate of the inductance can be made from the number of turns n, the mean radius a, and the outer radius r.

would be the case for an inductor with inner windings), L also decreases and thus it is clear that the inner windings of an inductor do not contribute to the total inductance. In fact, these windings reduce the total inductance. These hollow-core inductors have been shown to possess higher Q as compared to inductors containing inner windings [57], which is due to the increased parasitics that are introduced by these windings, as will be explained shortly. Therefore, hollow-core devices are certainly the most common planar topology found in the current research.

Now consider the cross-sectional perspective illustration of a simple planar IC inductor shown in Figure 4.9, where the equivalent electrical circuit is also superimposed. In this diagram, L is the total inductance, w is the width of the inductor trace, t is the thickness of the inductor trace, s is the distance between traces, ε_{ox} is the permittivity of the dielectric material, and t_{ox} is the thickness of the dielectric material between the bottom of the inductor and the top of the substrate. The parasitic elements include C_{ox} which is the dielectric capacitance, C_{si} which is the substrate capacitance, R_{si} which is the substrate resistance, and R_s which is the series loss in the inductor.

Expressions for each loss component are given in Table 4.1. In this table, ρ is the resistivity of the inductor material, δ is the skin depth, ω is the radian frequency, n is the
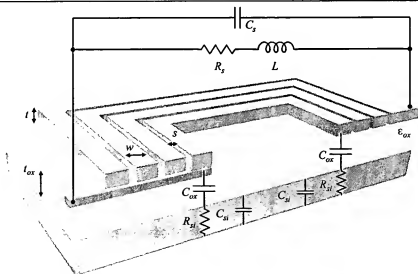
Figure 4.9   3D cross-sectional perspective illustration of a planar IC inductor with equivalent electrical circuit superimposed. Loss exists due to the series resistance, interwinding capacitance, and coupling into the substrate through C_{ox}.

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Parasitic variable	Loss mechanism	Expression
R_s	Loss due to series resistance and skin effect. Skin effect is a phenomena by which current is crowded around the surface of a conductor at high frequencies.	$R_S = \dfrac{\rho l}{w\delta(1 - e^{-t/\delta})}, \ \delta = \sqrt{\dfrac{2\rho}{\omega\mu_o}}$
C_s	Coupling between inductor traces due to physical proximity.	$C_S = nw\dfrac{2\varepsilon_{ox}}{s}$
C_{ox}	Coupling between the inductor and the substrate due to physical geometry of the dielectric material and inductor.	$C_{ox} = \dfrac{1}{2}lw\dfrac{\varepsilon_{ox}}{t_{ox}}$
C_{si}	Induced capacitance due to low resistance substrate.	$C_{si} = \dfrac{1}{2}lwC_{sub}$
R_{si}	Ohmic loss due to low resistance substrate.	$R_{si} = \dfrac{2R_{sub}}{lw}$

Table 4.1 Summary of loss mechanisms and corresponding expressions for a planar IC inductor.

number of turns, C_{sub} is a fitting parameter with units of capacitance per unit area, R_{sub} is a fitting parameter with units of resistance per unit area, and all other parameters are as defined previously.

The quality factor of the inductor can be expressed as a function of these parasitic elements. First consider the electrical model of the planar IC inductor again as shown in Figure 4.10a and consider a reduced and equivalent model, shown in Figure 4.10b, where,

$$R_P = \frac{1}{\omega^2 C_{ox}^2 R_{si}} + \frac{R_{si}(C_{ox} + C_{si})^2}{C_{ox}^2} \tag{4.3}$$

$$C_P = C_{ox}\frac{1 + \omega^2(C_{ox} + C_{si})C_{si}R_{si}^2}{1 + \omega^2(C_{ox} + C_{si})^2 R_{si}^2} \tag{4.4}$$

The reduction is introduced simply to provide some degree of simplicity to the expression for the device quality factor. After some extensive algebra, not shown here, the quality factor can be then given by,

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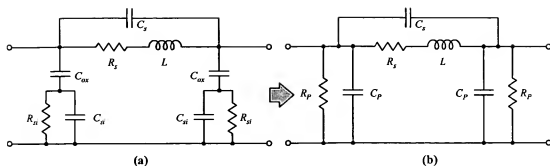
Figure 4.10 Equivalent circuit with parasitics for a planar IC inductor. (a) As modelled in Figure 4.9. (b) Simplified equivalent circuit for Q-factor calculation in (4.5).

$$Q = \frac{\omega L}{R_s} \left(\frac{R_P}{R_P + [(\omega L/R_s)^2 + 1]R_s} \right) \left(1 - \frac{R_s^2 C_P}{L_s} - \omega^2 L C_P \right) \tag{4.5}$$

where all variables are as defined previously. The first term in parenthesis in (4.5) can be described as a "substrate loss factor" because it represents loss to the substrate. The second term in parenthesis in (4.5) can be interpreted as a "self-resonance factor" because it models resonance phenomena with the parasitics. Lastly, the term $\omega L/R_s$ simply models the ohmic loss in the device.

From the model presented in Figure 4.10, the parasitics presented in Table 4.1, and the expressions in (4.2) and (4.5) it is clear where opportunities lie in order to improve the Q of a planar IC inductor. Approaches for reduction of these parasitics are summarized in Table 4.2 along with possible techniques. These techniques have been explored by many researchers and a breadth of approaches has been pursued and presented. These techniques are described for the remainder of this section.

One of the most obvious approaches is geometric optimization of the device for a fixed inductance. The work presented in [58], among many others, addresses this problem. In fact, a synthesis tool for inductors has been introduced in [59] and has become quite popular among RF design engineers. Additionally, investigations into the fundamental shape of inductors has also been explored. In [60] it has been shown that circular spiral inductors posses the best Q for a fixed L, largely due to minimized length for achieving the same L. Similarly, octagon inductors exhibit better Q than square inductors, but not better than cir-

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General enhancement approach	Specific enhancement approach	Implications, possible techniques
Reduce R_s	Increase t	Process determines t, increase t
	Increase δ	Process determines ρ thus δ, increase t or add low loss conductor
	Reduce l	L is reduced as l is reduced for fixed a and r, optimize
	Increase w	As w increases C_{ox} increases, optimize
Reduce C_s	Reduce n	Trade-off with n and r and a for same L, optimize
	Reduce w	As w decreases R_s increases, optimize
	Reduce ε_{ox}	Process determines ε_{ox}, remove dielectric or suspend device
	Increase s	As s increases so must l for the same L thus increasing R_s, NA
Reduce C_{ox}	Reduce l	L is reduced as l is reduced for fixed a and r, optimize
	Reduce ε_{ox}	Process determines ε_{ox}, remove dielectric or suspend device
	Increase t_{ox}	Process determines t_{ox}, NA
	Reduce w	As w decreases R_s increases, optimize
Reduce C_{si}	Reduce l	L is reduced as l is reduced for fixed a and r, optimize
	Reduce w	As w decreases R_s increases, optimize
	Reduce C_{sub}	C_{sub} determined by process substrate material, isolate it
Increase R_{si}	Increase R_{sub}	R_{sub} determined by process substrate material, isolate it
	Reduce l	L is reduced as l is reduced for fixed a and r, optimize
	Decrease w	As w decreases R_s increases, optimize

Table 4.2 Summary of enhancement approaches and techniques for a planar IC inductor. NA indicates that an enhancement technique is not available or not possible due to the implication listed.

cular inductors. Unfortunately, many modern CMOS processes do not support octagon or circular inductors due to the increased flash count that is required for mask fabrication.

Another interesting and recent approach to improving the performance of inductors involves the introduction of a patterned ground shield (PGS). This work was introduced in [61] and is a modification to the inductor structure that is completely CMOS compatible. In this approach, a metal or poly-silicon ground shield is placed under the inductor on the lowest metal layer, as illustrated in Figure 4.11. The shield is intended to isolate the lossy
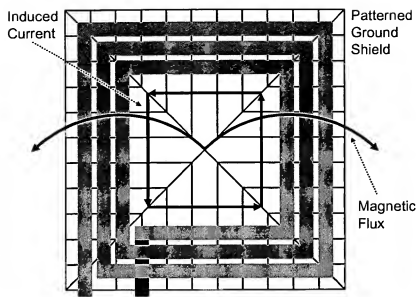
Figure 4.11 Hollow-core square spiral inductor with patterned ground shield. The direction of the magnetic flux is shown, along with the induced loop current. The ground shield is patterned orthogonally to the loop current in order to terminate it [61].

substrate from the inductor structure. The pattern is required in order to terminate the induced eddy current from magnetic flux as pictured in Figure 4.11. Here the patterned lines are perpendicular to the direction of the induced current. This minor modification to the inductor structure has been shown to increase the Q by as much as 30%. Effectively, the PGS eliminates C_{si} and R_{si}. However, it should be noted that the PGS increases C_{ox} because the PGS is fabricated on either the polysilicon layer or the first metal layer which are both substantially closer to the inductor than the substrate, particularly in the field. For example, for the *Taiwan Semiconductor*'s 0.18μm process, the top of the first metal layer is 21% closer to the inductor than the substrate [62], creating a corresponding increase in C_{ox}.

A completely alternative technique to realizing the inductor has been proposed and developed by several researchers in order to overcome the loss associated with skin effect and the series resistance. Inductor width or thickness must be increased to reduce series resistance. In this approach, the parasitic inductance of a bondwire is used in lieu of an integrated planar inductor [63]. A diagram illustrating this type of implementation is shown in Figure 4.12. Of course, the thickness of the bondwire inductor is substantially larger than

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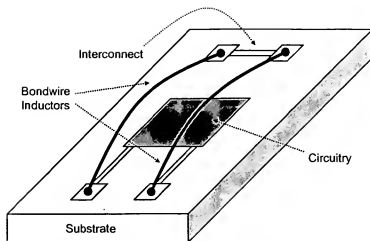
Figure 4.12 Bondwire inductors. Typically two wires are bonded across the substrate and then interfaced to the circuit. If the circuit is small, this area could be wasted.

the thickness of an integrated spiral inductor. Bondwire thickness is typically 25μm as compared to planar IC inductors, which are typically 2μm thick. As shown in [3], the inductance and loss of a bondwire can be estimated by the following relationships,

$$L \approx \frac{\mu_o l}{2\pi} \left[\ln\left(\frac{2l}{r}\right) - 0.75 \right] \qquad (4.6)$$

$$R_S = \frac{\rho l}{w\delta(1 - e^{t-/\delta})} \approx \frac{\rho l}{2r\delta} \qquad (4.7)$$

where r is the radius of the bondwire and all other terms are as defined previously.

Q factors up to 29 have been reported using this technique [63]. Although this is a clever approach, the inductance can be highly variable from bond to bond, thus jeopardizing frequency accuracy. Also, the area required for the bond wires is substantial and could increase the die size depending on the level of integration.

Another relatively obvious and popular approach is the use of a high resistance substrate under the inductor. For example, in *IBM's* 0.13μm SOI-CMOS 8SF process this technique is employed to decrease loss in the substrate. Also in this process, copper is utilized as the interconnect material [64]. The resistivity of copper is approximately 40% lower than

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aluminum [65] and therefore its use for the inductor structure reduces R_S by nearly the same amount and increases Q by approximately 50%.

A variety of high performance integrated inductors have also been demonstrated recently using micromachining technology and many of the reported devices possess a high Q-factor. For example, in [66] a copper-encapsulation technique has been demonstrated which yielded inductors with Q-factors over 30 at 5GHz. Several suspended approached have also been presented. In [67] a high performance suspended inductor using surface micromachined hinges was demonstrated where the inductor is raised 250μm over the substrate. Bulk micromachined approaches have also been demonstrated in [68], where the substrate is removed below the inductor. Other approaches that focus on reducing the coupling to the substrate include three-dimensional, as opposed to planar, implementations that are fabricated or self-assembled such that the magnetic flux is out of the substrate plane. In [74] an out-of-plane device has been shown to exhibit a Q-factor of 16.7 at 2.4GHz using a solenoid structure in electroplated copper. Other out-of-plane approaches that utilize hinges have been shown in [69], where good results have been demonstrated. A summary of this previous micromachined inductor work is presented in Table 4.3. Unfortunately, many of these micromachining approaches to the inductor problem are difficult to integrate

Ref.	Device	Nominal inductance	Q	Frequency	Year
[70]	Out-of-plane 3D self-assembled spiral	9nH	50	1GHz	2003
[71]	2D suspended	1.8nH	27	1GHz	2003
[68]	2D suspended	12nH	13.3	7.7GHz	2002
[72]	Out-of-plane 2D self-assembled spiral	4.5nH	12	1GHz	2002
[69]	Out-of-plane 2D self-assembled spiral	2nH	20	3GHz	2001
[73]	2D Cu-plated	2.6nH	17	2.5GHz	2001
[66]	2D Cu-encapsulated polysilicon	2-12nH	30	5GHz	2000
[74]	Out-of-plane 3D Cu solenoid	2.67nH	16.7	2.4GHz	1999
[75]	2D suspended	4.8nH	16	16GHz	1998
[76]	Out-of-plane 3D Cu coil	4.8nH	30	1GHz	1997
[67]	2D suspended in SOI	7.7nH	11	19.6GHz	1996

Table 4.3 Summary of previous micromachined inductor work.

Device topology	Nominal inductance	Process complexity	Accuracy	Q
Standard	1-25nH	No CMOS modification	Good	5-10
PGS	1-25nH	No CMOS modification	Good	7-12
Bondwire	1-25nH	No CMOS modification	Low	20-50
MEMS plated/encapsulated	2-25nH	High	Good	16-30
MEMS specialized 3D	~2-5nH	High	Moderate	15-30
MEMS suspended	1-25nH	Low to high	Good	11-16

Table 4.4 Qualitative and quantitative performance parameters for several inductor topologies.

with CMOS. Nevertheless, some insight can be gained upon examination of this previous work. Specifically, reduced substrate coupling can substantially increase the inductor quality factor. The challenge remains in maintaining CMOS-compatibility.

At this point it is appropriate to consider comprehensively the previous work in the area of integrated inductors, summarized in Table 4.4. The best technique for this research includes an inductor approach that provides good accuracy, high-Q, and low process complexity. Therefore, a combination of approaches has been identified for this work and includes use of a hollow-core planar topology, geometric optimization, a PGS, and some CMOS-compatible technique by which the inductor is suspended. The details of this approach and the associated design and fabrication will be presented in the following chapter.

4.2.2.2 Capacitors and Varactors

The capacitor or varactor serves as the electrical storage element within an electrically resonant harmonic reference. For this application, a varactor is required in order to tune the clock synthesizer to a prescribed accuracy. Several capacitor and varactor topologies are supported in nearly all modern IC fabrication processes. A review of these devices, including operation and performance, is presented here. It will be shown that a MEMS varactor presents one of the best opportunities for achieving high-Q and monolithic integration. However, some of the alternative solid-state devices that are described also present prom-

ising opportunities and warrant additional investigation beyond the work of this dissertation.

The simplest varactor device is the junction varactor. The device is shown conceptually in Figure 4.13a. It is constructed of a junction between oppositely doped semiconductor materials. A typical IC implementation is shown in Figure 4.13b where a lightly-doped well serves as one side of device and a heavily-doped diffusion region serves as the opposite side. Capacitance is realized by the depletion region that is created across the junction. The depletion region width, and corresponding capacitance, can be modulated by an applied bias. Of course, this bias must be applied in reverse across the junction because a forward bias would simply turn on the junction diode.

The capacitance across the junction can be estimated by assuming the junction is abrupt and possesses uniform doping on each side. It can be shown that under these assumptions, the junction capacitance is given by [77],

$$C = \varepsilon A \left[\frac{q}{2\varepsilon(V_o - V)} \left(\frac{N_A N_D}{N_A + N_D} \right) \right]^{1/2} \tag{4.8}$$
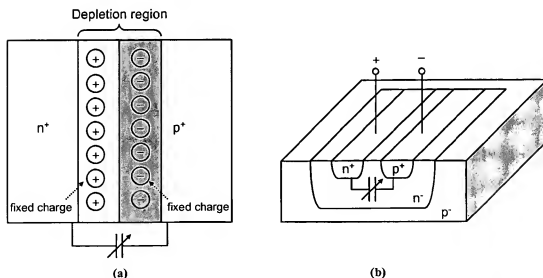
Figure 4.13 The p-n junction varactor. (a) Illustration of a conceptual p-n junction varactor. The capacitance is developed across the depletion region. (b) Perspective view of a practical implementation of a p-n junction varactor.

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where ε is the permittivity of silicon, A is the cross-sectional area of the junction, q is the magnitude of the charge on one electron, V_o is the built-in potential, V is the applied bias, N_A is the density of acceptors in the p-type region, and N_D is the density of donors in the n-type region. It is clear that the realized capacitance is nonlinear with applied bias. The expression in (4.8) can be reduced to the following,

$$C = \frac{A}{2}\left[\frac{2q\varepsilon}{V_o - V}N_D\right]^{1/2} \tag{4.9}$$

when the junction is doped asymmetrically, as shown in Figure 4.13b.

A charge carrier in a junction varactor must pass through a finite region of the well in order to reach the depletion region. Thus, the resistance associated with the junction varactor originates from the resistance of the lightly-doped well and the resistance of the diode. Typically, the latter is nearly infinite as long as the device is reverse biased. An estimate for the device's series resistance can be determined from the geometry of the junction and can be given by,

$$R = \frac{\rho_w L}{A} \tag{4.10}$$

where ρ_w is the resistivity of the well, L is the distance between the junction and the contact, and A is the cross-sectional area of the junction. For the asymmetrical junction, the Q-factor can be estimated by,

$$Q = \left|\frac{X}{R}\right| = \left|\frac{1/(j\omega C)}{R}\right| = \frac{1}{\rho_w L \frac{\omega}{2}\left[\frac{2q\varepsilon}{V_o - V}N_D\right]^{1/2}} \tag{4.11}$$

The Q is relatively stable throughout the reverse biased region, but it drops off very sharply once forward bias is approached due to the reduced parallel diode resistance, or equivalently an increase in parallel conductance. From (4.11) it is clear that device scaling will improve the quality factor where decreasing L increases Q.

Reported quality factors for this device vary greatly. For example in [78], a maximum Q-factor of 7 was reported. However, very recent results shown in [79] are even more

interesting where Q-factors ranging from over 100 to under 10 are reported for 0.5μm CMOS process technology. It is also worth noting that some high-Q junction varactors have been developed and presented recently and are constructed with hyperabrupt junctions. These devices are available commercially and offer Q-factors on the order of 1,000 or greater. However, these are discrete devices that have been manufactured with a specialized process. Therefore, they are not available to the CMOS designer. Nevertheless, the junction varactor has very recently become a viable option for this work and could be investigated further. However, the semiconductor junction varactor was not identified as the best option for this work primarily due to the large temperature sensitivity of this device.

Another device that is available in CMOS technology is the MOS varactor. The device can be constructed in the most general sense as shown in Figure 4.14a. Here, the capacitance is realized between the gate of an MOS device and the body. Typically the body, source, and drain are all connected to one potential and then the bias between that node and the gate modulates the capacitance. An alternate structure shown in Figure 4.14b, eliminates the drain and source, thus forcing the MOS capacitor to operate in accumulation mode and therefore the device is commonly called an A-MOS varactor.

The C-V characteristic behavior of a device such as this is shown in Figure 4.15. With the generalized structure, the device will exhibit a capacitance that varies through all MOS operating regions including accumulation, depletion, and the various degrees of
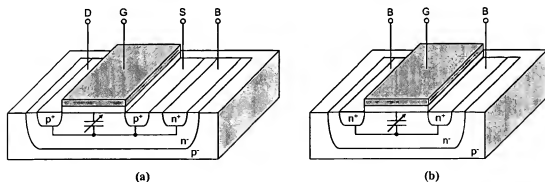
Figure 4.14   MOS varactors. (a) Generalized MOS varactor that operates in all MOS regions: accumulation, depletion, and inversion. Typically V_B, V_D, and V_S, are tied together and the bias is between that node and the gate. (b) Accumulation-mode MOS varactor. The bias is applied between the gate and the body.

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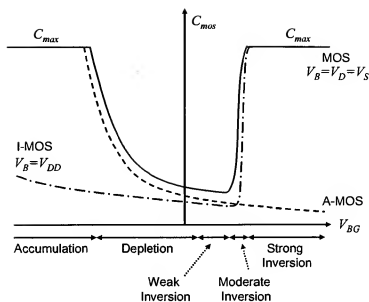
Figure 4.15 C-V characteristic of an MOS varactor. The general MOS varactor operates in all MOS regions. By forcing V_B to the highest voltage, inversion mode (I-MOS) can be maintained. Similarly, accumulation mode (A-MOS) can be forced using the topology in Figure 4.14b.

inversion. Of course, within the outlying regions, the capacitance is due simply to the intrinsic oxide capacitor, which is given by,

$$C = WLC_{ox} \tag{4.12}$$

where C_{ox} is the gate capacitance per unit area, W is the gate width, and L is the gate length.

By biasing the body to the highest potential, inversion mode (I-MOS) can be forced and the associated C-V characteristic is also shown in Figure 4.15. Alternately, the accumulation topology may be selected, as illustrated in Figure 4.14b, and the corresponding C-V characteristic is shown in Figure 4.15. The A-MOS device presents a broad and monotonic response as a function of bias voltage and thus this is often the topology of choice.

The small-signal resistance of the channel for a pMOS varactor in strong inversion has been derived in [80] and found to be,

$$R = \frac{L}{12k_p W(V_{GS} - V_{Tp})} \tag{4.13}$$

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where k_p is the gain factor of the pMOS transistor, V_{GS} is the voltage between the gate and the source/drain, and V_{Tp} is the threshold voltage for the pMOS transistor.

From this expression, the quality factor of the device can be evaluated as,

$$Q = \left| \frac{X}{R} \right| = \left| \frac{1/(j\omega C)}{R} \right| = \frac{12k_p(V_{GS} - V_{Tp})}{\omega C_{ox}L^2} \tag{4.14}$$

where ω is the radian frequency, and C_{ox} and W are as defined previously. Interestingly, the expression in (4.14) presents an opportunity to scale performance with process generation. Because Q is related to L inversely and quadratically, the Q-factor can be increased substantially for finer geometries. In [80] it has been shown theoretically that for a 0.8μm process, the Q-factor can be as large as 20 for a minimum length device and as high as 200 for a 0.25μm device.

These results, though very promising, have been derived with oversimplification of the MOS varactor. Although the complete analysis will not be presented here, it suffices to identify the errors in this analysis. First, minimum gate length devices are likely impractical because the realized capacitance would be too low for many applications. Just as tremendous gains can be realized with reducing L, significant loss in capacitance is realized by increasing L. Second, the device does not operate in strong inversion when the capacitance is modulated and therefore the analysis is not complete. An accurate model would include small-signal resistance through depletion and accumulation. Third, the series gate resistance and body resistance to the contact is certainly not negligible. In fact, it can be quite substantial. Consequently, typical Q-factors for this type of device can vary greatly with applied voltage and over frequency. Typical figures span values from less than 10 to over 100 as shown in [80].

Another significant problem is the fact that the MOS capacitance is highly variable over a range of bias conditions. For the clock synthesis application of this work, where large signal swings are required, the MOS capacitance may be difficult to predict or control, particularly as the device transitions into different regions of operation. Considering these observations along with the scaling issues just discussed, it is clear that the MOS varactor presents an interesting opportunity for use in an electrical harmonic reference. However, it

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Figure 4.16 MiM capacitor. The two metal plates are separated by a thin dielectric material. Typically, connection must be made by the next highest level of interconnect metal.

has not been identified as the most appropriate device for this work, but investigation of this device for future work is certainly warranted.

Another structure that is available in advanced CMOS processes is the metal-insulator-metal (MiM) capacitor. The device is simply two metal plates that are separated by a dielectric layer as shown in Figure 4.16. Typically the capacitor top-plate must be connected through the next highest interconnect metal as shown. The bottom plate is typically the next lowest metal layer. The capacitance of the device is set by the geometry and the material. Thus, by inspection, the device presents a nominal capacitance of,

$$C = \frac{\varepsilon A}{d} \tag{4.15}$$

where ε is the permittivity of the dielectric material, A is the top-plate area, and d is the distance between the plates.

The loss in this device is dominated by the series resistance associated with the top and bottom plates. Assuming the plates are the same size and that both the top and bottom plates are made of the same material, are the same thickness, and are square, the resistance can be expressed by,

$$R = R_t + R_b = \frac{2\rho}{t} = 2R_s \tag{4.16}$$

where R_t is the resistance of the top-plate, R_b is the resistance of the bottom-plate, ρ is the material resistivity, t is the layer thickness, and R_s is the sheet resistance. Using (4.16), the Q-factor of the device is simply,

$$Q = \left|\frac{X}{R}\right| = \left|\frac{1/(j\omega C)}{R}\right| = \frac{d}{\omega \varepsilon A 2 R_s} \tag{4.17}$$

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High Q-factors can be achieved with this structure. For example, MiM capacitors are supported in *Taiwan Semiconductor Manufacturing Company's* 0.18μm MM/RF process and the reported Q-factors are on the order of 30 and higher [62]. Also, the accuracy and temperature stability of these devices is quite high [62]. However, the most significant drawback associated with this structure is the fact that it is not tunable.

To overcome the low-Q that has been associated with early reports on the performance of variable junction and MOS varactors, much research has been pursued in the area of a tunable MiM varactor, or a micromachined varactor. In [81], one of the first parallel plate varactors was demonstrated with a tuning range of 16% and a nominal capacitance of 2pF. The device is basically a MiM structure with the dielectric material removed from between the plates. A moveable metal top plate is suspended over a fixed bottom plate and supported by a mechanical network of arms as shown in Figure 4.17, where an equivalent device is presented with a simpler support network as compared to that in [81]. By applying a voltage, V_{DC}, across the device, the moveable top plate will deflect some distance x. Thus, this voltage tunes the capacitance of the device. The details of this device's operation are presented next.
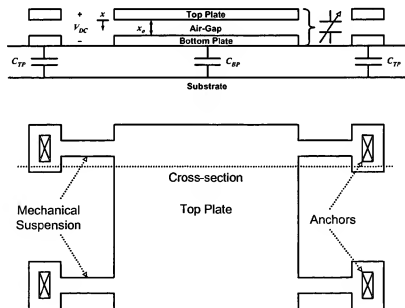
Figure 4.17 Cross-sectional and top views of a simple parallel-plate micromachined varactor. Parasitic capacitors C_{TP} and C_{BP} reduce the tuning range that can be achieved.

Recall that capacitance is given by the following relationship,

$$C = \frac{\varepsilon A}{x_o} \qquad (4.18)$$

where ε is the permittivity of air, A is the plate overlap area, and x_o is the nominal distance between the plates. Thus, for the varactor, this expression becomes,

$$C = \frac{\varepsilon A}{x_o - x} \qquad (4.19)$$

where x is some displacement forced by the tuning voltage. The electrostatic force generated between the plates by this voltage can be calculated by the following relationship:

$$F_e = \frac{1}{2}\frac{\partial C}{\partial x}V_{DC}^2 = \frac{1}{2}\frac{CV_{DC}^2}{(x_o - x)^2} \qquad (4.20)$$

The effective electrical spring constant is given by,

$$k_e = \left|\frac{\partial F_e}{\partial x}\right| = \frac{CV_{DC}^2}{(x_o - x)^2} \qquad (4.21)$$

A mechanical spring constant, k_m, is associated with the top plate suspension and a restoring force, F_m, is generated by this suspension. The relationship between k_m and F_m is given by Hooke's Law:

$$F_m = k_m x \qquad (4.22)$$

At equilibrium, the magnitudes of F_m and F_e are equal. From this condition, the relationship between the spring constants can be determined.

$$k_m x = \frac{1}{2}\frac{CV_{DC}^2}{(x_o - x)} = \frac{1}{2}k_e(x_o - x) \qquad (4.23)$$

Lastly, the expression for k_e in terms of k_m can be written as follows.

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$$k_e x = \frac{2k_m x}{(x_o - x)} \qquad (4.24)$$

Here it is interesting to note that when $x = x_o/3$, the two spring constants are equal. Beyond this point the electrical force exceeds the maximum mechanical restoring force and the plates are pulled together. The tuning voltage associated with a deflection of $x = x_o/3$ is called the pull-in voltage. Using this observation, the theoretical tuning voltage can be determined. First consider the nominal capacitance C_o,

$$C_o = \frac{\varepsilon A}{x_o} \qquad (4.25)$$

Now consider the maximum capacitance, C_{max}, which is for $x = x_o/3$,

$$C_{max} = \frac{\varepsilon A}{x_o - x_o/3} \qquad (4.26)$$

Lastly, solve for the tuning range using (4.25) and (4.26).

$$TR = \left| \frac{C_o - C_{max}}{C_{max}} \right| = \left| \frac{\frac{\varepsilon A}{x_o} - \frac{\varepsilon A}{x_o - x_o/3}}{\frac{\varepsilon A}{x_o}} \right| = \left| 1 - \frac{1}{2/3} \right| = \frac{1}{2} \qquad (4.27)$$

Thus, 50% tuning is the maximum range that can be achieved with this topology.

In Figure 4.17, C_{TP} and C_{BP} represent the parasitic capacitance to the substrate. These parasitic capacitors are what degrade the tuning range as shown in [81] and therefore 50% is difficult to achieve. Having identified this problem, a modified MEMS varactor topology was introduced in [82] and a tuning range of 69.8% was achieved. The modification introduced is illustrated in Fig. 4.18. Here the control voltage is applied across a large gap while the tunable section of the varactor is across a small gap.

Another MEMS varactor was demonstrated in [83] with a tuning range of 300% using lateral comb structures which were fabricated using a deep reactive ion etch (DRIE)
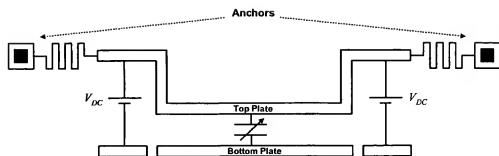
Figure 4.18 High tuning range varactor. The electrostatic force is applied by a voltage across a large gap while the capacitance is realized across a small gap.

technique in SOI. However, these devices pose significant integration challenges with standard CMOS processing and consequently are not appropriate for monolithic applications.

Varactors even more exotic than these have been developed recently, such as those presented in [84]. In this work, rather than modify the distance between two parallel plates, a dielectric is moved into and out of the region between the plates. This device has been reported with a very impressive Q-factor of 291. Again, though, this device is quite difficult to integrate into a CMOS process.

Table 4.5 summarizes these devices and other previous work in the area of micromachined varactors. These MEMS devices present some of the most promising opportunities for realizing a monolithic reference technology. High Q-factors and reasonable tuning ranges can be achieved in a small silicon area. Additionally, these devices are quite simple and typically are not constrained by concerns pertaining to power dissipation, signal swing, or bias. However, process complexity is still of concern and must be addressed.

Ref.	Topology	Tuning range	Nominal capacitance	Q	Frequency	Year
[84]	Parallel plate with moveable dielectric	7.7%	1.14pF	291	1GHz	2000
[82]	Modified parallel plate	69.8%	58fF	NA	NA	2000
[83]	Comb	300%	1-5pF	100	400MHz	1998
[81]	Parallel plate	16%	2pF	60	1GHz	1997

Table 4.5 Summary of previous micromachined varactor work.

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Device topology	Achievable tuning range	Typical capacitance/area	Achievable Q	Accuracy
PN Junction	50%	NA	4-200	Moderate
MOS	50%	NA	4-200	Moderate
MiM	0%	1fF/μm^2	30-100	Good
MEMS	15%-300%	0.2fF/μm^2	30-300	Good

Table 4.6 Summary of capacitor and varactor performance for various device topologies.

Table 4.6 lists the performance parameters for all of the varactor devices that have been discussed in this section. MEMS presents the most promising opportunity and specifically a parallel-plate MEMS varactor has been identified as the most appropriate device for this work because it provides high-Q and a reasonable tuning range within an acceptable silicon area. Additionally, the parallel-plate device is relatively simple as compared to other MEMS varactor topologies. Thus a CMOS-compatible integration approach can likely be developed and such an approach is presented in the following chapter.

Although the parallel-plate MEMS varactor has been selected for this work, it is worthwhile to refer to [78] again where junction and MOS varactors were reported with a Q of only 7, as described previously. MiM capacitors were reported in this same work with Q-factors up to 36. In fact, in [78] it is stated that MiM capacitors are clearly a superior choice over MOS or junction devices. The only cited drawback is the increased area required for MiM caps. This drawback has been mitigated by the fact that CMOS processes that support MiM devices now utilize a very thin dielectric layer in order to increase the capacitance per unit area. A more significant and current observation pertains to the Q-factor performance improvements achieved and reported recently for junction and MOS varactors. Much of the MEMS varactor work that was pursued was based on reports like those in [78]. Consequently, a solution for a tunable and high-Q MiM structure was sought. Now it appears that the performance gains realized through the use of this structure are not nearly as great as originally believed due to advances in junction and MOS varactor research. Nevertheless, MiM structures still do posses certain inherent advantages. For example, a junction varactor must be designed such that it never enters forward bias, while

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this constraint does not apply to MEMS varactors, thus offering some design flexibility. Also significant variation in MOS and junction varactor performance has been reported and is largely dependent on process technology. In contrast, MEMS varactors have all been reported with high-Q performance. Lastly, achieving accuracy can be a challenge with MOS and junction varactors while MEMS varactors have been reported with quite good accuracy. Nevertheless, it is clear that future research could be pursued in the area of junction and MOS devices as they pertain to this work.

4.3 High-Performance Monolithic Oscillators

Given the level of research activity in the area of monolithic reference devices, it is only natural that a wide variety of monolithic oscillators have been reported recently. Here, an overview of this recent work is presented. First, it is instructive to discuss some qualitative and quantitative metrics. A variety of technologies are presented in the data that follow and include process technologies that are not CMOS as well as reference technologies that are not yet monolithic, but likely could be in the near future. These are included in order to present opportunities in the field that have not yet matured fully, such as MEMS resonator technology. It should also be noted that work reported in BiCMOS or bipolar cannot be directly compared to the CMOS work because of the substantial difference in the noise characteristics of the bipolar and MOS active devices.

Quantitative figures of merit include phase noise PSD, power dissipation, and oscillation frequency. Much of the current work in the field is reported over a broad range of these metrics and thus a composite figure-of-merit (*FOM*) is commonly employed in order to facilitate direct comparison of the performance of published work. This *FOM*, first proposed in [85], is given by,

$$FOM = \left(\frac{N_o}{P_o}\right)_{f_m} - 20\log\left(\frac{f_o}{f_m}\right) + 10\log\left(\frac{P_{DC}}{1\,mW}\right) \qquad (4.28)$$

where $(N_o/P_o)_{f_m}$ is the phase noise PSD at offset f_m, f_o is the fundamental frequency, and P_{DC} is the power dissipated in the oscillator. The *FOM* is typically a negative number near

-200. The more negative the number, the better the performance. The *FOM*, along with other performance metrics are summarized in Table 4.7 on the next page.

Clearly, some of the best performance to date has been achieved with the use of MEMS as the reference device. For example, using the *FOM*, the best four designs all made use of MEMS. However, it is also worth noting that some of these oscillators have not yet been demonstrated entirely in monolithic form. For example, the work in [86] utilized a micromachined varactor on a separate chip which was bonded to the active CMOS circuitry. Though this is a multi-chip approach, it could ultimately be integrated in the future.

It is certainly important to analyze and develop high-quality reference devices for oscillators, but the application must also be considered thoroughly throughout the development of the reference. The most significant observation that can be gained from investigation of Table 4.7 is that MEMS oscillators have demonstrated the best performance to date. However, some of these devices have been presented with challenges. For example, the microresonator-based oscillator in [54] has been reported with excellent close-to-carrier phase noise, but due to the nonlinear transduction of the reference device, the phase noise at even modest offset frequencies is quite poor. Interestingly, the microresonator utilized in [54] possesses a *Q*-factor of over 5,000. This example illustrates that consideration for the end application is the most significant aspect of any engineering problem. Based on device performance, this microresonator is an excellent choice. But in an oscillator, the large feedback signal and nonlinear transduction nearly make this reference device unusable. In this light, Table 4.7 is presented as a final sanity check that the identified reference devices are appropriate for the clock synthesis application of this work. Clearly electrically resonant references dominate the prior research and good results have been reported for devices that are similar to those that have been developed in this dissertation.

4.4 Conclusions

A variety of oscillator reference technologies have been reported to date. Many of the most interesting and promising have been presented here. MEMS reference devices present the most promising opportunity for realizing a high-performance monolithic oscillator. Previous research has been presented on the performance of these devices both as individual cir-

Ref.	Technology (reference device, process)	Phase noise PSD	Power	Freq.	*FOM*
[70]	3D out-of-plane ind. + MiM capacitor, BiCMOS + micromachining post-process	-111dBc/Hz @ 100kHz	11mW	1.2GHz	-182*
[71]	Suspended ind. + MOS varactor, CMOS + micromachining post-process	-117dBc/Hz @ 300kHz	15mW	2.6GHz	-184*
[71]	Suspended ind. + MOS varactor, CMOS + micromachining post-process	-124dBc/Hz @ 300kHz	15mW	1GHz	-183*
[99]	Integrated planar ind. + junction varactor, Bipolar	-140dBc/Hz @ 3MHz	35mW	1.6GHz	-179
[54]	MEMS microresonator, CMOS wire bonded to MEMS	-80dBc/Hz @ 1kHz	NA	9.8MHz	NA
[87]	Post-processed Cu ind. + junction varactor, Bipolar + micromachining post-process	-106dBc/Hz @ 100kHz	18mW	2GHz	-179*
[88]	Integrated planar ind. + junction varactor, Bipolar	-104dBc/Hz @ 100kHz	14mW	2.6GHz	-181
[89]	Integrated planar ind. + junction varactor, BiCMOS	-125dBc/Hz @ 600kHz	34mW	2GHz	-180
[86]	Bondwire ind. +MEMS varactor, CMOS wire bonded to MEMS	-126dBc/Hz @ 600kHz	15mW	1.9GHz	-184*
[86]	Bondwire ind. + MEMS varactor, CMOS wire bonded to MEMS	-122dBc/Hz @ 1MHz	14mW	2.4GHz	-178*
[90]	Integrated planar inductor + varactor diode, BiCMOS	-129dBc/Hz @ 3MHz	18mW	2.4GHz	-175
[91]	Integrated planar ind. + junction varactor, Bipolar	-139dBc/Hz @ 4.7MHz	30mW	1.8GHz	-176
[92]	Integrated planar ind. + junction varactor, SOI-CMOS	-110dBc/Hz @ 1MHz	3mW	2GHz	-171
[93]	Bondwire/integrated ind. + junction varactor, CMOS	-126dBc/Hz @ 600kHz	13mW	1.1GHz	-180
[94]	Bondwire ind. + MOS varactor, CMOS	-119dBc/Hz @ 600kHz	12mW	1.3GHz	-175
[81]	Integrated planar ind. + MEMS varactor, CMOS wire bonded to MEMS	-105dBc/Hz @ 100kHz	NA	1GHz	NA
[95]	Integrated planar Cu ind. + varactor diode, BiCMOS	-122dBc/Hz @ 600kHz	21mW	1GHz	-173
[81]	3D out-of-plane ind. + MEMS varactor, CMOS wire bonded to MEMS	-136 dBc/Hz @ 3MHz	43mW	859MHz	-169*
[96]	MEMS microresonator, CMOS-MEMS	-88dBc/Hz @ 500kHz	NA	1MHz	NA
[57]	Integrated planar ind. + junction varactor CMOS	-116 dBc/Hz @ 600kHz	6mW	1.8GHz	-178
[97]	Bondwire ind. + junction varactor CMOS	-115 dBc/Hz @ 200kHz	28mW	1.8GHz	-180

Table 4.7 **Summary of recent monolithic and multi-chip MEMS oscillator work. MEMS work is indicated by an asterisk. NA = not available.**

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cuit components and as the reference for an oscillator. Although a variety of mechanical and electrical MEMS references have been presented successfully, an electrically resonant MEMS reference has been identified as the most appropriate device for this research. This selection has been motivated largely by the ability to achieve CMOS integration and high performance with minimal process complexity. Performance includes high-Q, good accuracy, and the ability to tune the reference in order to improve accuracy. The identified reference device includes an optimized planar hollow-core suspended inductor with a PGS coupled with a parallel-plate MEMS varactor derived from the standard CMOS MiM structure. The design and fabrication details for these devices will be discussed in the following chapter.

CHAPTER V

A 900MHZ MONOLITHIC AND TOP-DOWN CLOCK

SYNTHESIZER WITH MICROMACHINED RADIO

FREQUENCY REFERENCE

Several key concepts were presented in the previous chapters as background and motivation for the development of the clock synthesis approach that is described within this chapter. An overview of oscillator topologies was presented in Chapter II and the complementary cross-coupled configuration was selected as the best option for achieving monolithic integration with low phase noise. In Chapter III, the concept of a top-down system architecture was introduced and the details of such an implementation are discussed in this chapter. An overview of state-of-the-art monolithic reference technologies and oscillators was presented in Chapter IV. It was determined that an electrically resonant and micromachined LC oscillator presented the best opportunity for integration with CMOS and with the selected oscillator topology. In all, these chapters have laid the foundation for the fundamental design considerations associated with the clock synthesis approach that has been developed and prototyped in this work.

This chapter opens with a discussion of the target manufacturing process for prototyping, which is critical in two senses. First, the fabrication process must be compatible with standard processes for fabricating microcontrollers and microprocessors. Second, it must support the development of the reference technology for the oscillator. The discussion that follows addresses both of these issues. The chapter continues with the theoretical design of the oscillator reference. Test performance from an array of fabricated devices is presented. Some challenges were faced in the development of the MEMS varactor device

and thus an alternate approach to achieve frequency tuning is proposed and demonstrated. The chapter continues with the theoretical design of the oscillator. Theoretical predictions are compared with simulation data and measured data from fabricated devices. A summary of these theoretical, simulation, and measured results is presented and analyzed. Lastly, the chapter closes with a discussion of future research topics based on the results obtained.

5.1 Target Fabrication Process

The vast majority of the microprocessors and microcontrollers fabricated in the world today are fabricated in a CMOS process. Thus, without any doubt, CMOS must be the fabrication process of choice for this work. Moreover, a modern and fine resolution process technology is certainly more desirable because of the CMOS processors that exist, the vast majority are developed in fine geometry processes. Moreover, as process generations scale to finer geometries, additional challenges arise with the design of analog and RF circuits. Thus a successful design in such a process truly validates this work since first, it can be deployed into current processor systems and second, the challenges associated with fine geometry processes are addressed.

Given the myriad of goals outlined in the previous chapters, some advanced process options are certainly desirable. In fact, such options are now becoming standard for many CMOS foundries due to the emergence of SoC and microsystem development. As described in Chapter I, designers pursuing SoC and microsystem development are merging logic with analog and RF functions. Therefore, the options associated with analog and RF design have found their way into mainstream CMOS. One such process is the 0.18μm mixed-mode/radio-frequency (MM/RF) process available from *Taiwan Semiconductor Manufacturing Company* (*TSMC*). This process offers three key options that are utilized in this work. First, a metal-insulator-metal (MiM) capacitor structure is supported and a modified rendition of it has been designed in order to explore the development of a small-gap MEMS varactor. Second, the process supports a thick top metal layer that is ideal for the suspended inductor proposed in Chapter IV. Lastly, a deep *n*-well option allows nMOS and pMOS devices to be fabricated in wells that are isolated from the substrate. This minimizes noise injection into the clock synthesizer which can originate from the switching of the

nearby processor logic. The details of how the CMOS fabrication process plays an instru-
mental role in all of these aspects is described in the following sections.

For now it suffices to note that a mixed-mode CMOS process from any foundry pre-
sents a viable option for prototype development of this work. However, it is also worth
noting that although the options just described are attractive, they are not mandatory. In fact
the MiM structure described in this work could be fabricated from the standard CMOS
interconnect layers, but with a significant increase in silicon area due the difference in spac-
ing between the two layers. In fact, such designs are also explored in this work. Similarly,
without the thick top metal option for the inductor, the Q of the LC-tank is simply degraded
and thus the short term stability of the clock would also be degraded. Lastly, without the
deep n-well option, noise could couple into the synthesizer and decrease the stability of the
clock signal. Thus, the selected fabrication process presents the best available opportunity
when considering performance. However, it is certainly not the only opportunity. This fact
becomes significant when considering a port of this work to alternate manufacturing pro-
cesses. Indeed, it can be achieved, but likely with performance degradation. Nevertheless,
some techniques can be employed in order to overcome the degradation just described. For
example, inductors can be fabricated by tying multiple interconnect layers together in pro-
cesses where the thick top metal option is unavailable. This approach reduces the Q degra-
dation due to increased ohmic loss from reduced metal thickness.

5.2 Reference: A High-Q CMOS-Compatible Micromachined LC-Tank

The MEMS technology in this work includes a suspended inductor and a micromechanical
varactor. Together, these components comprise a high-Q LC-tank which serves as the elec-
trical harmonic reference for the clock oscillator. A significant focus of this work has been
to develop these components in a manner that is compatible with commercial CMOS man-
ufacturing processes. Specifically, a simple maskless post-process has been developed to
release the micromachined components after completion of the standard CMOS manufac-
turing process. Moreover, the components have been designed such that the structural
layers of each device are defined by the existing interconnect layers in the standard CMOS
process. Previous work, as shown in Chapter IV, was developed with elaborate post-pro-

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cessing or complicated custom CMOS processes that included fabrication of MEMS components within the process flow. In other more related work such as that in [98], the use of CMOS interconnect and dielectric stacks has been demonstrated in the development of high-aspect-ratio microstructures. In contrast to previous work, the work in this dissertation has been focussed at the development of RF MEMS components using a simple maskless fabrication post-CMOS process where devices are constructed from the interconnect metal layers and released from the interconnect dielectric material.

5.2.1 Suspended Inductor

The standard inductor available in the *TSMC* process provides good performance, but by removing the dielectric material around it, the performance can be improved, as described in Chapter IV. Removing the dielectric material reduces the capacitance between the structure and the substrate, thus reducing the loss due to induced eddy current by magnetic flux and ultimately improving the Q of the device. Additionally and in conjunction with this approach, the use of a PGS is explored.

5.2.1.1 Improvement on Start-of-the-Art

Many suspended inductor designs have been presented, the most notable of which were summarized Chapter IV. This work has not been focussed at exclusively maximizing the Q of the inductor. Rather, in this application, the goal is to increase the Q of the inductor structure in the simplest and least expensive manner possible while maintaining commercial CMOS compatibility. In this sense, this approach improves the state-of-the-art because most previous approaches required complicated and expensive processing steps, some of which were not CMOS-compatible.

5.2.1.2 Fabrication Process

The suspended inductor is fabricated as a standard inductor in the last and thick metal layer in *TSMC*'s 0.18µm MM/RF process. However, two posts are fabricated using the metal and dielectric stack from first metal to last metal. These posts support the structure after release. Next, an overglass cut, which is the standard layer used for bond pad exposure, is placed

around the inductor structure. Thus, the last standard manufacturing step involves removing the passivation nitride around the inductor. With the cut made, a maskless wet etch can be performed in order to remove the silicon dioxide below the inductor. The rest of the circuit is protected from this sacrificial etch by the silicon nitride passivation layer, which does not etch in the presence of most oxide etchants and is, in fact, quite difficult to remove in general [100]. In contrast, the stack dielectric is silicon dioxide and thus it can be selectively etched with no additional mask layer.

The sacrificial etch is performed with Pad Etch IV, a commercial etchant that removes silicon dioxide in the presence of aluminum (Al). The typical application for this etchant is to open the bond pad contacts in a standard CMOS process and hence the corresponding name. The interconnect material and the metal that defines the inductor structure in this work is aluminum and of course it is of utmost importance to protect these layers during the post-processing. For this reason, standard oxide etchants such as hydrofluoric acid (HF) cannot be utilized.

Pad Etch IV is a buffered acetic acid (CH_3COOH) solution containing 12-16% ammonium fluoride (NH_4F), and 51-55% water (H_2O). It is manufactured by *Ashland Specialty Chemical Company* (now *Air Products*). The chemical etches CMOS passivation oxide (typically phosphosilicate glass or PSG) that is deposited by chemical vapor deposition (CVD). The etch rate is approximately 4000Å/min. at room temperature [101]. In contrast, only minimal etching of Al is observed as shown in [102]. The etch was performed for 15 minutes, which corresponds to removal of approximately 6μm of dielectric material. Lateral etch, which certainly occurs, is of no significance because the design rule for the inductor structure in *TSMC* requires that the inductor be placed 50μm from any active device. The trench is constructed to be larger than periphery of the inductor but at least 10μm away from neighboring structures on all sides. Thus, it is impossible for the post-process to compromise the reliability of any of the neighboring electronics.

Both a cross-sectional perspective illustration of the final structure is shown in Figure 5.1. Here the overglass cut can be observed, which creates a trench around the inductor structure. The subsequent wet etch deepens and widens this trench, the latter of which

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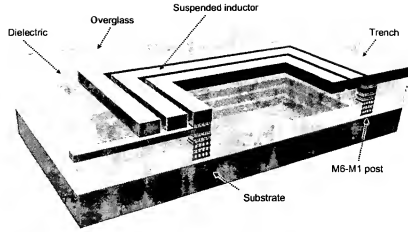
Figure 5.1   Perspective illustration of a cross-section of the fabricated suspended inductor.

is due to lateral etching. The silicon nitride overglass layer protects the interconnect on the rest of the integrated circuit and prevents etching anywhere away from the trench.

5.2.1.3 Theoretical Design and Simulation Results

As shown in Chapter IV, the nominal inductance of the device can be determined from the device geometry. With the use of a first order model, the inductance can be estimated by the following relationship [3],

$$L \approx \frac{37.5\mu n^2 a^2}{22r - 14a} \tag{5.1}$$

where a is the mean radius of the spiral, n is the number of turns, μ is the permeability of the core, and r is the outer radius of the spiral.

TSMC also provides empirical relationships, based on measurements from fabricated devices, in order to determine the inductance [62]. These expressions are given below for the case where $R = 60\mu m$ in (5.2) and $n = 4.5$ in (5.3),

$$L \approx 0.4042n^2 - 0.995n + 2.3295 \tag{5.2}$$

$$L \approx 0.0916R + 0.7461 \tag{5.3}$$

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where n is the number of turns and R is the inner radius of the spiral. Note that R in (5.3) is different from r in (5.1) because the latter corresponds to the outer radius of the spiral. Using these relationships, an empirical estimate of the nominal inductance can be determined by fixing either R or n and taking the ratio of the inductance for the remaining design variable to the inductance for $R = 60\mu m$ or $n = 4.5$.

Three inductor structures were designed and prototyped, all having different nominal inductance values. In each case the standard, suspended, and suspended with a PGS structures were designed. All designs were targeted for 900MHz operation. The Q-factor of the device at this frequency was estimated theoretically using (4.5). A summary of these device design parameters is given in Table 5.1 on the following page.

5.2.1.4 Measured Performance

A die micrograph of the prototype chip is shown in Figure 5.2. This die contains renditions of both the inductor and varactor structure. Measurement results from the latter will be presented in the next sections. Figure 5.3 is a scanning electron micrograph (SEM) of the 10nH
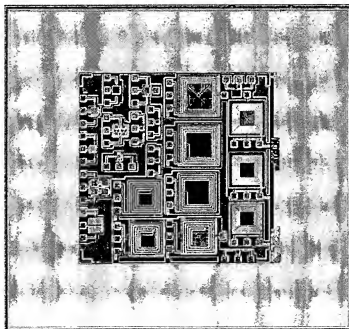
Figure 5.2   Die micrograph of the suspended inductor and micromechanical varactor prototype integrated circuit in *TSMC*'s 0.18μm MM/RF process.

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Design parameter	6nH design	8nH design	10nH design
Target inductance (L)	6nH	8nH	10nH
Theoretical inductance (L)	5.60nH	7.57nH	9.95nH
Empirical inductance (L)	6.04nH	7.64nH	10.9nH
Topology (all square hollow core)	a. Standard b. Suspended c. Suspended/PGS	a. Standard b. Suspended c. Suspended/PGS	a. Standard b. Suspended c. Suspended/PGS
Frequency (f_o)	900MHz	900MHz	900MHz
Resistivity (ρ)	28.3nΩ-m	28.3nΩ-m	28.3nΩ-m
Skin depth at f_o (δ)	2.82μm	2.82μm	2.82μm
Dielectric permittivity (ε_{ox})	a. 3.9 b. ~1 c. ~1	a. 3.9 b. ~1 c. ~1	a. 3.9 b. ~1 c ~1
Distance between inductor and substrate/PGS (t_{ox})	a. 8.15μm b. 8.15μm c. 6.4μm	a. 8.15μm b. 8.15μm c. 6.4μm	a. 8.15μm b. 8.15μm c. 6.4μm
Fitting parameter (C_{sub})	10^{-14}fF/m^2	10^{-14}fF/m^2	10^{-14}fF/m^2
Fitting parameter (R_{sub})	$10^{-5}\Omega$/m^2	$10^{-5}\Omega$/m^2	$10^{-5}\Omega$/m^2
Shunt resistance (R_P)	a. 7.21kΩ b. 104kΩ c. ∞	a. 7.70kΩ b. 111kΩ c. ∞	a. 11.1kΩ b. 160kΩ c. ∞
Shunt capacitance (C_P)	a. 102fF b. 27.7fF c. 0.138pF	a. 95.9fF b. 25.9fF c. 0.129pF	a. 66.6fF b. 18.0fF c. 897fF
Series loss (R_s)	4.04Ω	5.91Ω	9.24Ω
Interwire coupling (C_s)	a. 23.3fF b. 5.97fF c. 5.97fF	a. 13.3fF b. 3.40fF c. 3.40fF	a. 8.84fF b. 2.27fF c. 2.27fF
Substrate coupling (C_{ox})	a. 108fF b. 27.8fF c. 0.138pF	a. 101fF b. 26.0fF c. 0.129pF	a. 70.5fF b. 18.1fF c. 897fF
Substrate capacitance (C_{si})	2.56×10^{-22}F	2.39×10^{-22}F	1.66×10^{-22}F
Substrate ohmic loss (R_{si})	391Ω	419Ω	601Ω
Trench overhang	a. No trench b. 8μm c. 8μm	a. No trench b. 12μm c. 12μm	a. No trench b. 27μm c. 27μm
Length (l)	3410μm	3990μm	4160μm

Table 5.1 Design parameters for standard, suspended, and suspended with PGS inductor designs.

Design parameter	6nH design	8nH design	10nH design
Number of turns (n)	4.5	4	6
Mean radius (a)	96.125μm	126.25μm	87.75μm
Radius (r)	132.75μm	152.5μm	115.5μm
Hollow core radius (R)	60μm	100μm	60μm
Thickness (t)	2μm	2μm	2μm
Width (w)	15μm	12μm	8μm
Turn spacing (s)	1.5μm	1.5μm	1.5μm
Device material	Al	Al	Al
Theoretical Q-factor at f_o	a. 7.96 b. 8.38 c. 8.22	a. 6.85 b. 7.25 c. 7.08	a. 6.28 b. 6.62 c. 6.46

Table 5.1 Design parameters for standard, suspended, and suspended with PGS inductor designs.

inductor structure after the release. It can be seen that the trench around the inductor has deepened and the field is unaffected. The inductor itself appears to be only slightly etched as indicated by the surface roughness seen in the SEM.
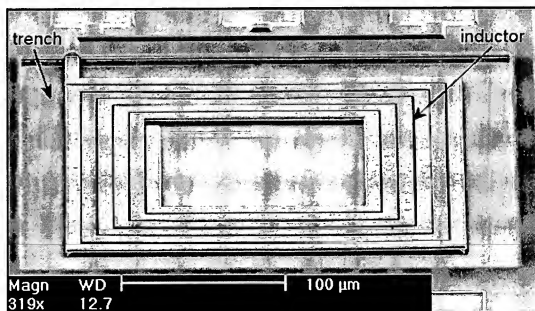
Figure 5.3   Electron micrograph of the 10nH suspended inductor after a 15 minute wet etch with Pad Etch IV. Some etching of the inductor material is observed. No etching of the field is observed.

Test measurements were acquired by probing the die using a *Cascade Microtech* RF-1 microwave probe station and 40GHz air coplanar probes with a 100μm pitch ground-signal ground configuration (ACP-40-GSG-100). The wafer chuck was grounded, thus grounding the backside of the die and the substrate. An *Agilent* 8753ES vector network analyzer and *Agilent's Intuilink* GPIB software were used to capture the data. The short-open-load (SOL) technique was used to calibrate the ACP-40 probes and the corresponding correction factor was applied internally in the 8753ES. An open probe pad structure was measured in order to de-embed the S_{11} parameters of the device under test from the electrical parasitics associated with the probe pads. To do this, S_{11} parameters were converted to admittance parameters using the following relationships [103],

$$Y_R = \frac{1}{Z_R} \text{ and } Z_R = Z_o \frac{(1 + S_{11})}{(1 - S_{11})} \tag{5.4}$$

Once converted, the parasitic admittance values can simply be subtracted from the measured admittance parameters of the device under test. Figure 5.4 shows the de-embedded S_{11} measurements for all inductor structures on a Smith chart. Each chart contains data for the standard, suspended, and suspended with PGS structures for each of the three target inductance values. Higher Q is indicated by a larger radius from the origin.

The Q-factor can be calculated over frequency by the following relationship,

$$Q = \left| \frac{Im(Y_R)}{Re(Y_R)} \right| \tag{5.5}$$

where $Im(Y_R)$ and $Re(Y_R)$ designate the imaginary and real components of the complex reflection admittance, Y_R. The Q-factor over frequency for each design and topology is shown in Figure 5.4.

Results show that the Q was degraded in the suspended with PGS designs when compared to the standard inductor structure. This is due to the that fact that C_{ox} is increased by the presence of the PGS because the distance between the inductor and the ground plane is reduced by the presence of the PGS. Clearly, the PGS approach is not appropriate for the inductor sizes in this work. However, it can be shown that for very small inductor sizes, the
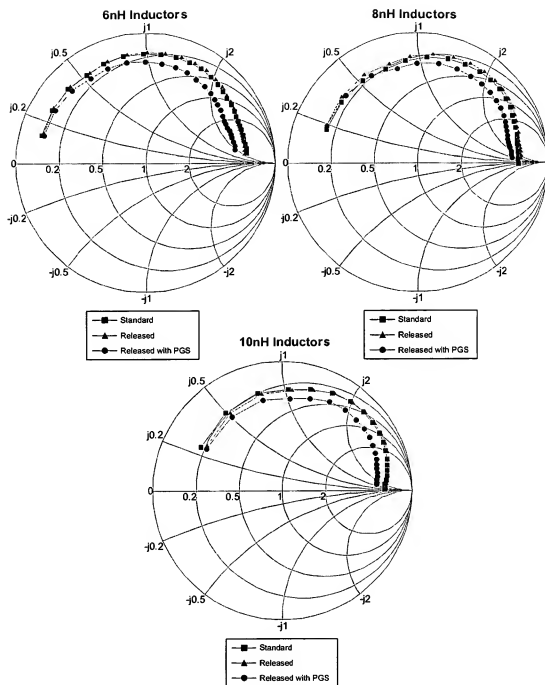
Figure 5.4   Measured and de-embedded S_{11} for all inductor designs. (a) 6nH. (b) 8nH. (c) 10nH.

PGS technique works well [58]. Results also show that the Q was increased for both the 6nH and 8nH suspended designs. However, the Q was decreased for the 10nH design. The latter is due to the fact that the 10nH design possesses the smallest trace width. Thus, the Q
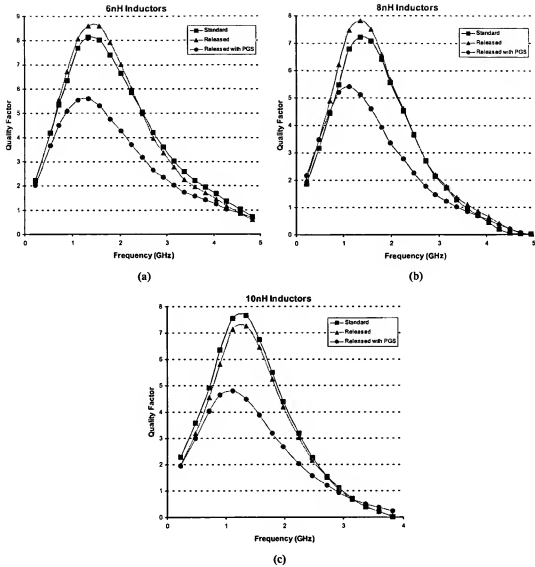
Figure 5.4   Q-factor measurements over frequency for each topology and each inductance. (a) 6nH. (b) 8nH. (c) 10nH.

of this design was limited by the ohmic loss associated with the inductor and not the loss due to the substrate. Therefore, the trench etching had little effect on the performance of this design. It is likely that during the etch, some of the inductor material also etched and therefore the Q was reduced. As for the other two designs, the maximum that the Q was increased was 7.3% for the 6nH design and 13.2% for the 8nH design. These differences are due to the differences in the trench size. The trench overhang in 8nH design was 12μm, while it was 8μm for the 6nH design. The results at 900MHz for Q are summarized in

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Design	Theor. Q at 900MHz	Meas. Q at 900MHz	Theor. L at 900MHz (nH)	Emp. L at 900MHz (nH)	Meas. L at 900MHz (nH)	Theor./Emp. L accuracy
6nH	a. 7.96 b. 8.38 c. 8.22	a. 6.35 b. 6.71 c. 5.08	5.60nH	6.04nH	5.96nH	-6%/1.3%
8nH	a. 6.85 b. 7.25 c. 7.08	a. 5.49 b. 6.22 c. 4.49	7.57nH	7.64nH	7.64nH	-0.92%/0.0%
10nH	a. 6.28 b. 6.62 c. 6.46	a. 6.36 b. 5.81 c. 4.65	9.95nH	10.90nH	11.11nH	-10%/1.9%

Table 5.2 Comparison of theoretical and measured quality factor and theoretical, empirical, and measured inductance for all inductor designs at 900MHz.

Table 5.2 along with theoretical, empirical, and measured results for inductance and the associated accuracy.

5.2.1.5 Discussion

A simple wet etch post process has been demonstrated successfully as a technique by which the inductor Q-factor can be increased. In contrast, the popular PGS technique has been demonstrated to decrease the Q-factor for the designed inductors, which is due to the increase in C_{ox} because of the decreased distance between the PGS and the inductor as compared to the distance between the inductor and substrate without the PGS. It can be shown that this PGS technique is appropriate only for small inductor values [58].

Although this approach does not deliver performance that rivals the results from some of the more exotic previous work, it is comparable to the original reports using the PGS as presented in [61], which has now become a popular inductor design technique for small inductor sizes. Thus, the approach presented here may also become similarly popular, although this approach differs fundamentally because there is no lower or upper inductance bound in its application.

Another observation not to be overlooked in the data is the inductance accuracy. Worst case empirical inductance inaccuracy for this prototype run was less than 2%. This fact will become critical in the design of the reference oscillator for this work as the inductance is one of the key components that sets the oscillator frequency. Of course, achieving

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high frequency accuracy is a critical metric as described in Chapter II. As for future work, more exact tolerances for the inductance accuracy could be obtained by collecting data across multiple designs and multiple process runs.

5.2.2 Micromechanical Varactor

5.2.2.1 Improvement on State-of-the-Art

Several micromechanical varactors of various topologies have been presented in Chapter IV, most of which were fabricated by a specialized process apart from CMOS. Other, more recent work, has shown MEMS varactors merged with CMOS using a MEMS over CMOS post-process [104]. In contrast, this is the first work demonstrating RF MEMS in commercial CMOS where the structure is defined by the standard CMOS interconnect layers and a simple maskless post-process can be used to release the device. Additionally, the development of very small-gap varactor structures is pursued in this work, along with more typical large-gap structures. The small-gap varactor is of interest because the nominal capacitance can be realized within a small area and consequently microphonic sensitivity is decreased greatly due to the reduction in associated mass as compared to a large-gap structure. Unfortunately, these small gap devices were not demonstrated successfully in this work for reasons that will be shown in the following sections.

5.2.2.2 Fabrication Process

In order to achieve monolithic integration, it was imperative that the varactor fabrication process be compatible with the inductor fabrication process described previously. In fact, this goal was relatively simple to achieve. It was determined that two renditions of the micromechanical varactor could be developed in a compatible process. The small-gap rendition can be realized by releasing the dielectric material between the plates of the standard metal-insulator-metal (MiM) capacitor. Similarly, the large-gap rendition can be developed by releasing the dielectric between the top two interconnect metals, or metal 5 (M5) and metal 6 (M6). Moreover, both of these devices can be etched with the same etch that is utilized to suspend the inductor. All that is required is a similar overglass cut.

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As described in Chapter IV, the MiM structure is fabricated with a specialized layer that is within close proximity to the previous interconnect layer, thus realizing a high capacitance per unit area. Connection to the specialized layer is achieved by a via connection from the subsequent interconnect layer. The goal, then, is to release the dielectric material between the specialized layer and the previous interconnect layer. In the *TSMC* process the specialized layer is M5' and the previous interconnect layer is M5. The M5' layer is connected by the sixth metal layer, M6. In order to accommodate the release, etch windows were included in both the M6 and M5' layers. Of course, because the etch is simply timed and the overglass trench will be deepened substantially during the release process, the M5 bottom plate must be supported in some fashion. This was achieved by placing support posts in each of the four corners of the bottom plate. A perspective illustration of the varactor realized from this MiM capacitor is shown in Figure 5.5. The M5-M6 rendition is identical except that the gap spacing is larger.

It is important to note that in the case of the inductor, the release etch simply increases the Q-factor of the device, but it does not change the nominal inductance. In the case of the varactor, the capacitance changes substantially because the relative dielectric constant prior to etching is 3.7. After the etch, this constant becomes approximately 1 and thus the capacitance is reduced by a factor of 3.7 after the etch. Like the inductor structures, the etch was timed for 15 minutes, where approximately 6μm of PSG was expected to be removed.
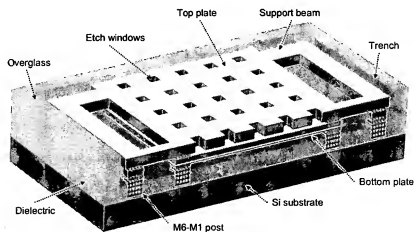
Figure 5.5   Perspective illustration of a cross-section of the micromachined varactor.

Development of a varactor around the MiM structure is quite aggressive and for this reason, large-gap varactors fabricated from the M5 and M6 interconnect layers are also developed in this work. A varactor realized from these two interconnect layers will have a much lower capacitance per unit area and thus require much more area while also making the device more susceptible to microphonics. This is, of course, undesirable but the M5-M6 varactor is much easier to release because of the larger gap.

5.2.2.3 Theoretical Design and Simulation Results

The micromechanical varactor in this work is of a parallel-plate topology similar to that presented in [81] and it is illustrated in Figure 5.6. The operation of this device was presented in Chapter IV. Here, a more extensive theoretical derivation of the behavior of the device is derived. The nominal capacitance of the device is given by,

$$C = \frac{\varepsilon A}{x_o - x} \qquad (5.6)$$

(a)

(b)
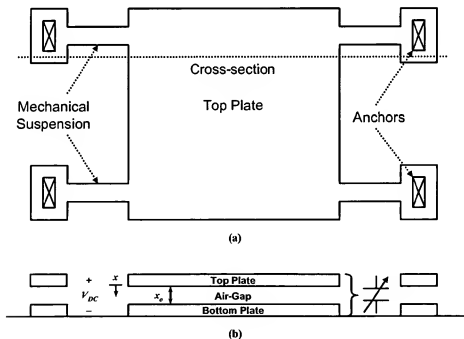
Figure 5.6 A parallel-plate RF MEMS varactor. (a) Top view illustrating the mechanical suspension network. (b) Cross-section illustrating device operation by electrostatic actuation.

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where ε is the permittivity of air, A is the plate overlap area, x_o is the nominal distance between the plates, and x is some displacement forced by the DC tuning voltage, V_{DC}. It has been shown in Chapter IV that the maximum displacement for this topology is $x_o/3$, beyond which the electrical force exceeds the maximum mechanical restoring force and the plates are pulled together.

Now consider the electrostatic force, F_e, generated between the plates by the applied tuning voltage, V_{DC}. F_e can be derived by considering the energy, E, stored between the plates.

$$F_e = \frac{\partial E}{\partial x} = \frac{1}{2}\frac{\partial C}{\partial x}V_{DC}^2 = \frac{1}{2}\frac{CV_{DC}^2}{(x_o - x)} \tag{5.7}$$

A mechanical spring constant, k_m, is associated with the top plate suspension. A mechanical restoring force, F_m, is created by this suspension. The relationship between k_m and F_m is given by Hooke's Law:

$$F_m = k_m x \tag{5.8}$$

The magnitudes of F_m and F_e are the same at equilibrium as the electrostatic force is balanced by the mechanical restoring force of the suspension network. Therefore, using (5.7) and (5.8) gives the following.

$$k_m x = \frac{1}{2}\frac{CV_{DC}^2}{(x_o - x)} \tag{5.9}$$

Finally the relationship between V_{DC} and x can be expressed using (5.9).

$$V_{DC} = \sqrt{\frac{2k_m x(x_o - x)^2}{\varepsilon A}} \tag{5.10}$$

From (5.10), the pull-in voltage can be determined. It has already been shown that the maximum displacement is $x = x_o/3$. Thus, the pull-in voltage is given by,

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$$V_{pull-in} = \sqrt{\frac{2k_m(x_o/3)(x_o - x_o/3)^2}{\varepsilon A}} = \sqrt{\frac{8k_m x_o^3}{27\varepsilon A}} \tag{5.11}$$

The only remaining parameter to determine is the mechanical spring constant, k_m, which can be determined simply from geometry. The general expression is [105],

$$k_m = \frac{\beta E w t^3}{L^3} \tag{5.12}$$

where β is a configuration dependent parameter, E is Young's modulus, w is the width of the supporting beam, t is its thickness, and L is its length. For the geometry shown in Figure 5.6, $\beta=4$.

Lastly, the Q-factor of the device can be determined by solving for the resistance of the top and bottom plates. For a square varactor (ignoring the etch holes), this is given by,

$$R_{top} = \frac{\rho}{t_{top}} \text{ and } R_{bot} = \frac{\rho}{t_{bot}} \tag{5.13}$$

and the Q can be determined by,

$$Q = \left| \frac{Im(Z_{11})}{Re(Z_{11})} \right| = \frac{1/\omega C}{R_{top} + R_{bot}} \tag{5.14}$$

A design approach involves first determining the process specific parameters and then determining the design variables. Process specific parameters include Young's modulus (E), the varactor gap (x_o), and the support beam thickness (t), thus leaving the remaining variables for design: nominal capacitance (C_o), pull-in voltage ($V_{pull-in}$), support beam topology parameter (β), support beam length (L), and the support beam width (w). Several of these design variables are dependent on each other. Thus, the best approach is to determine the most critical parameters which are certainly the nominal capacitance and the pull-in voltage. Once a nominal capacitance is selected (5.6) can be solved for A for the case $x = 0$. Next, (5.11) can be used to determine k_m for a given pull-in voltage. Lastly, topology determines β and the support width and length can be found by selecting an appropriate width and solving for length using (5.12).

Figure 5.7   Illustration of FEA of electrostatic actuation of the varactor.

The MiM varactor was designed using this approach and then verified with the finite element analysis (FEA) tool, *Coventorware*. Figure 5.7 shows an image of an electrostatic FEA of the device. The color contours indicate relative displacement, x, from the nominal position, x_o. The figure represents the results of a coupled electromechanical simulation where top-plate displacement is forced by an applied voltage.

The design parameters for both the MiM and M5-M6 varactors are given in Table 5.3 on the following page. Due to die size constraints, the support beam length was restricted and thus the M5-M6 varactor requires a large tuning voltage. Without these constraints, the support beam length could have been increased in order to realize a more appropriate pull-in voltage.

5.2.2.4 Measured Performance

A die micrograph of the prototype devices was shown previously in Figure 5.2, where both varactor and inductor structures are included. A scanning electron micrograph (SEM) of a 2-by-2 MiM varactor array is shown in Figure 5.8. It can again be seen that the trench around the varactor array has deepened and the field is unaffected. Figure 5.9 shows a close-up of the varactor gap for both the MiM and the M5-M6 varactors. It can be seen in Figure 5.9a that the MiM dielectric material did not etch at all. However, in Figure 5.9b it can be seen that all of the M5-M6 dielectric material is completely etched, except for the MiM dielectric material. This remaining material between the M5-M6 varactor is so small, that is does not affect operation of the device. Thus, the M5-M6 varactor is functional and, unfortunately, the MiM varactor cannot be operated.

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Design parameter	MiM	MiM	M5-M6	M5-M6
a. Pre-rel. cap. (C_o) b. Post-rel. cap. (min/max)	a. 875fF b. 225fF/337fF	a. 3.5pF b. 897fF/1.35pF	a. 140fF b. 33fF/50fF	a. 560fF b.133fF/200fF
Topology	Parallel-plate	Parallel-plate	Parallel-plate	Parallel-plate
Array size	1	4	1	4
Topology parameter (β)	4	4	4	4
a. Pre-rel. rel. perm. (ε_r) b. Post-rel. rel. perm. (ε_r)	a. ~3.7 b. ~1	a. ~3.7 b. ~1	a. ~4.2 b. ~1	a. ~4.2 b. ~1
Frequency (f_o)	900MHz	900MHz	900MHz	900MHz
Gap distance (x_o)	32.8nm	32.8nm	772nm	772nm
Overlap area (A)	875μm^2	3500μm^2	2907μm^2	11,628μm^2
Support beam length (L)	11μm	11μm	11μm	11μm
Support beam width (w)	4μm	4μm	1μm	1μm
Support beam thickness (t_{top})	2.34μm	2.34μm	2.34μm	2.34μm
Bottom-plate thickness (t_{bot})	0.53μm	0.53μm	0.53μm	0.53μm
Mech. spring constant (k_m)	10.8kN/m	10.8kN/m	14.5kN/m	14.5kN/m
Resistivity (ρ)	28.3nΩ-m	28.3nΩ-m	28.3nΩ-m	28.3nΩ-m
Device material	Al	Al	Al	Al
Young's modulus (E)	70GPa	70GPa	70GPa	70GPa
Pull-in voltage ($V_{pull-in}$)	3.8V	3.8V	121V	121V
Tuning range (TR)	50%	50%	50%	50%

Table 5.3 Design parameters for MiM and M5-M6 micromachined varactor prototypes. Two
renditions of each were designed where one rendition is a 2-by-2 array of the baseline
varactor.

It appears that the MiM dielectric is not strictly silicon dioxide but rather a mix of
silicon dioxide and silicon nitride, also known as oxy-nitride. This material is very difficult
to etch [100], particularly in the presence of aluminum. In fact, as described in previous sec-
tions, the passivation layer in CMOS is typically silicon nitride or oxy-nitride. The resis-
tance of this material to a broad variety of etch chemistries laid the foundation for the
maskless post-process etch proposed in this work. Alternate etch chemistries for the MiM
dielectric have been investigated but no appropriate chemistry has been identified to date.
Thus, results from only the M5-M6 varactors are reported here.
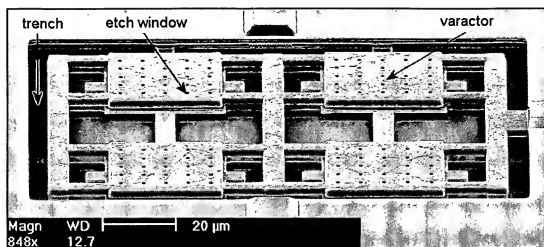
Figure 5.8   Electron micrograph of the 2-by-2 MiM micromechanical varactor array.

Test measurements were acquired using the same set-up used for inductor testing. The die was probed using a *Cascade Microtech* RF-1 microwave probe station and air coplanar probes (ACP) with a 100μm pitch. An *Agilent* 8753ES vector network analyzer was used to capture the data. The short-open-load (SOL) technique was used to calibrate the ACP-100 probes and the corresponding correction factor was applied internally in the 8753ES. Again, admittance measurements from an open probe pad were used to de-embed the measured parameters. Figure 5.10 shows the S_{11} measurements of the 2-by-2 M5-M6 varactor after release. The measured Q of the device was approximately 60 at 900MHz. This Q is substantially higher than the Q of the inductor presented previously at the fre-

(a)   (b)
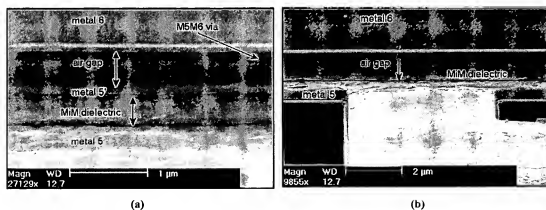
Figure 5.9   Electron micrograph of the micromechanical varactor gap. (a) The MiM rendition where the MiM dielectric material is not etched. (b) The M5-M6 rendition where all of the dielectric material except the MiM dielectric is etched.

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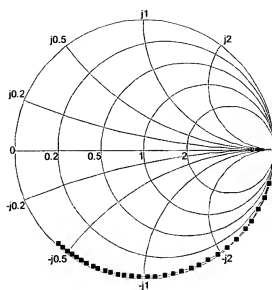
Figure 5.10 Measured and de-embedded S_{11} parameters of the 2-by-2 M5-M6 varactor array after release.

quencies of interest. Thus, the inductor limits the performance of the reference and in subsequent analyses, only the inductor Q need be considered.

The tuning response of the devices was determined by applying a DC voltage through a bias tee and detecting the capacitance with the 8753E network analyzer at 900MHz. This test set-up is shown in Figure 5.11 and the measured DC tuning response for both M5-M6 varactors is shown in Figure 5.12 along with the theoretical response. Unfortunately, due to the very high spring constant associated with the varactor top-plate support
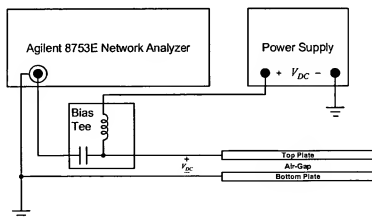
Figure 5.11 Test set-up for determining the varactor tuning range.

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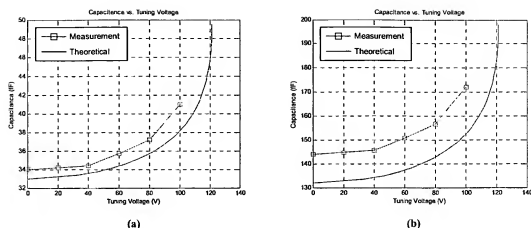
Figure 5.12 Measured and theoretical tuning range of M5-M6 micromechanical varactors (a) Single varactor. (b) 2-by-2 array.

network, the required DC tuning voltage is unreasonably high. Around 100V, arching between the two metal plates is observed and measurements can no longer be made. Despite this set-back, the varactor capacitance does change with the applied bias and follows a response similar to the theoretical behavior, at least within the operational range of the device, as shown in Figure 5.12.

5.2.2.5 Discussion

This work is one of the first reports of micromechanical varactors in commercial CMOS where the devices are defined by the standard interconnect layers and release is achieved by a maskless post-process. The MiM small-gap rendition was nonfunctional due to the fact that the gap could not be etched. However, the M5-M6 rendition was developed successfully. The measured device Q was approximately 60 at 900MHz and the measured tuning range was approximately 20%, which was limited due to the arching phenomenon seen at high tuning voltages. The measured nominal capacitance was in error from the theoretical values by 3%. As with the inductor, the accuracy achieved is significant because it indicates the frequency accuracy that can be attained. Of course, more accurate tolerance could be determined from tests across several manufacturing runs.

The fact that an etch chemistry for the small-gap MiM varactor could not be developed presented an engineering challenge as well as some redirection to this work. Although

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the M5-M6 varactor was functional, the required device size for even a modest capacitance is prohibitive for fine geometry CMOS processes. Moreover, these large devices cause the clock synthesis system to be more sensitive to microphonics. Of course the clock synthesizer could certainly be developed with these M5-M6 varactors, but the associated performance drawbacks are too many.

Considering these factors, the primary function of the varactor in this work was investigated again. The varactor serves the purpose of tuning the clock frequency in order to achieve increased frequency accuracy as compared to the clock frequency accuracy that is achieved out of fabrication. Modulating the reference capacitance provides a simple mechanism by which the frequency can be tuned quite easily. The purpose of the MEMS varactor was to provide this tuning mechanism while maintaining high Q. As shown in Chapter IV, junction and MOS varactors typically do not posses the same performance. Of course, a completely alternate approach could be pursued, such as varying the inductance. However, this is quite difficult. Beside these two approaches, there does not exist an obvious frequency tuning technique. However a simple systemic method by which this can be achieved without varying either the inductance or capacitance does exist. The frequency pulling term introduced in (2.123) can be tuned electrically by varying the effective loss, R. This technique does not provide nearly as broad of a tuning range as the varactor would, but it does provide enough of a range to achieve very high frequency accuracy. Thus, this systemic approach is employed for the developed clock synthesis system and it is described in greater detail in the following sections. The developed design does, however, also support the varactor structures for the event that an etch chemistry is developed and these structures can be released. Additionally, the suspended inductor structure, which was introduced in the previous sections, is also utilized in this work and enhancements are made based on the test results from the previous sections.

5.3 Low-Phase-Noise and Low-Power RF Core

A survey of circuit topologies was presented in Chapter II and the complementary cross-coupled configuration was selected for this work for primarily two reasons. First, this topology provides the best opportunity for integration with the LC components just described.

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Second, it has been shown that the double symmetry of the circuit promotes waveform symmetry which has been shown to improve phase noise performance. In the sections that follow, this oscillator topology is thoroughly analyzed within the context of the critical metrics presented in Chapter II.

5.3.1 Start-Up Analysis

A schematic of the complementary cross-coupled amplifier topology is shown in Figure 5.13a. This amplifier is one from a class of amplifiers commonly referred to as negative resistance amplifiers. As described in Chapter II, a negative resistance amplifier can be used to effectively cancel the loss in the tank and thus ensure oscillation. The negative resistance realized by this configuration can be determined from small signal analysis of the circuit, shown in Figure 5.13b, where the finite output resistance has been ignored and the transconductance of all of the devices is assumed to be identical. Of course the pMOS and nMOS devices must be sized appropriately relative to each other in order for the latter con-

(a)   (b)
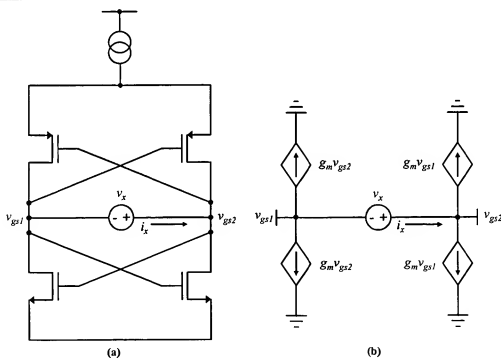
Figure 5.13   Determining the negative resistance realized by the complementary cross-coupled amplifier. (a) Transistor-level schematic with test voltage indicated. (b) The small-signal equivalent circuit where output resistance has been ignored.

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dition to hold. The resistance across the circuit can be determined by applying a test voltage across the terminals and determining the current response. Referring to Figure 5.13b and by applying Kirchoff's current law, the test current is given by the following.

$$i_x = -g_m v_{gs2} - g_m v_{gs2} = g_m v_{gs1} + g_m v_{gs1} \tag{5.15}$$

$$i_x = -2g_m v_{gs2} = 2g_m v_{gs1} \tag{5.16}$$

From (5.16), it is clear that the small-signal voltages are always equal and opposite, as specifically given in (5.17).

$$-v_{gs1} = v_{gs2} \tag{5.17}$$

Because the test voltage is applied across the terminals of the circuits, its value is given by (5.18).

$$v_x = v_{gs2} - v_{gs1} = v_{gs2} + v_{gs2} = 2v_{gs2} \tag{5.18}$$

Substituting (5.18) into (5.16) gives.

$$i_x = -2g_m v_{gs2} = -g_m v_x \tag{5.19}$$

From (5.19), the input resistance is given by (5.20).

$$\frac{v_x}{i_x} = R_{in} = -\frac{1}{g_m} \tag{5.20}$$

Therefore the realized negative resistance is $-1/g_m$ and the transconductance of the amplifier is simply $-g_m$. From here, two approaches can be used to determine a condition for start-up. The first and simplest approach is to utilize the Barkhaussen magnitude criterion. If the tank has a parallel loss of R_P, then for this oscillator topology, the Barkhaussen magnitude criterion becomes,

$$g_m R_P > 1 \tag{5.21}$$

which gives rise to the design constraint,

$$g_m > \frac{1}{R_P} \tag{5.22}$$

R_P represents the parallel loss in the tank and thus the more loss, the lower R_P becomes, thus requiring more transconductance and effectively more power in order to maintain the oscillation.

Another satisfying approach that leads to the same conclusion involves using the notion of the negative resistance. Consider the loss R_P in parallel with the sustaining amplifier that presents a negative resistance of R_{amp}. In the ideal case, R_{amp} is exactly equal to R_P and the equivalent parallel resistance is infinite.

$$\lim_{|R_{amp}| \to R_P} \left[\frac{1}{\frac{1}{R_P} - \frac{1}{|R_{amp}|}} \right] = \infty \tag{5.23}$$

Substituting the expression for $|R_{amp}|$ with $1/g_m$ gives,

$$\lim_{\frac{1}{g_m} \to R_P} \left[\frac{1}{\frac{1}{R_P} - \frac{1}{\frac{1}{g_m}}} \right] = \infty \tag{5.24}$$

From (5.24) and the notion of negative resistance, it is clear that the negative resistance must be at least as negative as the loss in the tank. Using this fact and the denominator of the expression in (5.24), the following condition is determined,

$$\frac{1}{R_P} - \frac{1}{\left| \frac{1}{g_m} \right|} \leq 0 \tag{5.25}$$

from which the following is determined,

$$g_m \geq \frac{1}{R_P} \tag{5.26}$$

which is identical to the expression in (5.22). Typically R_{amp} is determined by selecting an integer overdesign factor such that $R_{amp} = R_p/A$ where A is an integer greater than one, thus ensuring the magnitude start-up criterion is met. The notion of the overdesign factor will be used throughout the remainder of this Chapter.

Next it is instructive to consider the effects of transconductance mismatch on the start-up condition. Equation (5.15) can be rewritten for the case that the pMOS devices have transconductance g_{mp} and the nMOS devices have transconductance g_{mn}. The expression becomes,

$$i_x = -g_{mp}v_{gs2} - g_{mn}v_{gs2} \qquad (5.27)$$

Using (5.18), (5.27) can be rewritten as,

$$i_x = \frac{-g_{mp}v_x}{2} - \frac{g_{mn}v_x}{2} \qquad (5.28)$$

and finally the negative resistance is given by,

$$\frac{v_x}{i_x} = R_{in} = -\frac{2}{g_{mp} + g_{mn}} \qquad (5.29)$$

where it is clear that the expression in (5.20) is obtained for the case where $g_{mp} = g_{mn}$. Mismatch is not of much concern because the realized negative resistance is simply the sum of the transconductance from each device. However, mismatch will certainly affect waveform symmetry and thus, for this reason, it is desirable to match the transconductance of the pMOS and nMOS devices as closely as possible.

Lastly, it is worthwhile to consider the effect of finite output resistance on the realized negative resistance. The small-signal circuit in Figure 5.13b can be redrawn to include this resistance as shown in Figure 5.14a. This circuit can be simplified to the circuit shown in Figure 5.14b, where it is assumed that the nMOS and pMOS transconductance values match as do the lengths of all of the devices such that the output resistance is the same. Applying Kirchoff's current law, the test current is given by,

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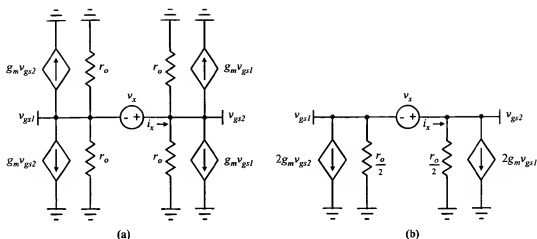
Figure 5.14 Small-signal model of the complementary cross-coupled negative resistance amplifier including transistor output resistance. (a) Schematic from transistor implementation. (b) Reduced schematic for analysis.

$$i_x = -2g_m v_{gs2} - \frac{v_{gs1}}{r_o/2} \tag{5.30}$$

$$i_x = 2g_m v_{gs1} + \frac{v_{gs2}}{r_o/2} \tag{5.31}$$

Adding (5.30) and (5.31) gives,

$$2i_x = -2g_m(v_{gs2} - v_{gs1}) + \frac{1}{r_o/2}(v_{gs2} - v_{gs1}) \tag{5.32}$$

The test voltage, v_x, is given by $v_x = v_{gs2} - v_{gs1}$ and thus,

$$2i_x = -2g_m v_x + \frac{2}{r_o}v_x = v_x\left(-2g_m + \frac{2}{r_o}\right) \tag{5.33}$$

$$R_{in} = \frac{v_x}{i_x} = \frac{1}{-g_m + \frac{1}{r_o}} \tag{5.34}$$

Therefore the output resistance of the transistor degrades the amount of negative resistance that is realized. Of course the expression in (5.34) becomes equal to (5.20) in the limit as r_o approaches infinity, or specifically,

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$$\lim_{r_o \to \infty} \left[\frac{2}{-2g_m + \frac{1}{r_o/2}} \right] = -\frac{1}{g_m} \qquad (5.35)$$

This result presents a design trade-off since r_o is increased by increasing the length of the transistors, but g_m is increased by the ratio of the transistor width to the transistor length. Therefore if the length is increased, the width must also be increased in order to achieve the same transconductance, which may result in an unreasonably large transistor aspect ratio. These observations are taken into account in the detailed design section of this dissertation.

5.3.2 Oscillation Frequency, Tuning Range, and Sensitivity Analysis

5.3.2.1 Exact Oscillation Frequency

In Chapter II, the exact oscillation frequency was determined by solving the time-domain differential equations for a harmonic LC tank with loss. The solution is,

$$\omega_r = \sqrt{\omega_o^2 - \alpha^2} \qquad (5.36)$$

where $\omega_o = (\sqrt{LC_{eq}})^{-1}$ and $\alpha = (2RC_{eq})^{-1}$. C_{eq} is the total capacitance in the tank, including the capacitance contributed by the amplifier. R is the total loss in system including the loss in the tank and the loss due to the loading of the amplifier. These loss components contribute to the phenomenon called frequency pulling, as described in Chapter II and as is apparent from the expression in (5.36). It will be shown that the systemic frequency pulling effect is the dominant cause of frequency sensitivity to power supply variation. First, an exact expression for the oscillation frequency is derived. Then a detailed sensitivity analysis can be conducted.

The generalized complementary cross-coupled oscillator shown in Figure 5.13a is typically configured as shown in Figure 5.15a such that the tank capacitance can be realized with varactors and then tuned at the midpoint, which is indicated as an AC ground in Figure 5.15a. Of course, the amplifier also contributes a large capacitance to the total tank capac-

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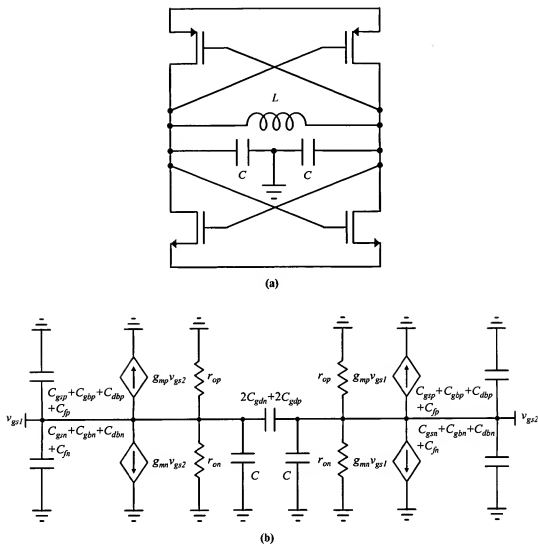
Figure 5.15 AC analysis schematic of the complementary cross-coupled LC oscillator. (a) Transistor schematic. (b) Small-signal equivalent circuit.

itance as shown in the small-signal equivalent circuit given in Figure 5.15b, which can be simplified to the schematic shown in Figure 5.16a. An equivalent circuit including these capacitors can be drawn as shown in Figure 5.16b. Here C represents each side of the tank capacitors, C_p represents the MOSFET capacitors that are in parallel with the tank, and C_D represents the MOSFET drain capacitors that are in parallel with the tank capacitors. Noting that the ground is a common node, as in Figure 5.16a, the equivalent capacitor, as shown in Figure 5.16b, is given by,

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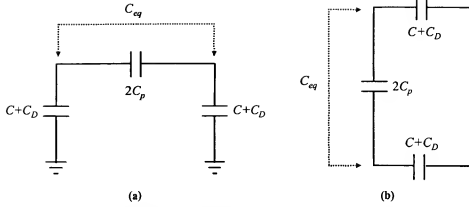
Figure 5.16 AC schematic of equivalent tank capacitance. (a) From the schematic in Figure 5.15b. (b) After reduction of the circuit in (a).

$$C_{eq} = 2C_p + \frac{C + C_D}{2} \tag{5.37}$$

Referring to Figure 5.15b, the parallel capacitor is given by,

$$C_p = C_{gdn} + C_{gdp} \tag{5.38}$$

where C_{gdx} indicates the gate-to-drain capacitance of a device with polarity x, given by $C_{gdx} = C_{GDO_x} W_x$ where $CGDO_x$ is the gate-to-drain overlap capacitance per unit gate length and the W_x is the transistor width.

Similarly, C_D can be determined from inspection of Figure 5.15b.

$$C_D = C_{fn} + C_{gsn} + C_{gbn} + C_{dbn} + C_{fp} + C_{gsp} + C_{gbp} + C_{dbp} \tag{5.39}$$

C_{fx} represents the gate fringing capacitance for a device of polarity x which is the sum of the inner and outer fringe components, indicated by C_{if} and C_{of} respectively and given by [106],

$$C_{fx} = C_{if_x} + C_{of_x} = \frac{2\varepsilon_{si}W_x}{\pi}\ln\left(1 + \frac{x_j}{2t_{ox}}\right) + \frac{2\varepsilon_{ox}W_x}{\pi}\ln\left(1 + \frac{t_{gate}}{t_{ox}}\right) \tag{5.40}$$

where W is the width of the transistor, ε_{si} is the permittivity of silicon, x_j is the drain/source junction depth, t_{ox} is the gate oxide thickness, and t_{gate} is the gate poly thickness.

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C_{gsx} represents the gate-to-source capacitance for a device of polarity x. This capacitance is due to both overlap and a capacitance to the channel when the device is in strong inversion as given by,

$$C_{gsx} = CGSO_x W_x + \frac{2}{3} W_x L_x C_{ox}$$ (5.41)

where $CGSO_x$ is the gate-to-source overlap capacitance per length for a device of polarity x. C_{ox} is the oxide capacitance per unit area as given by $C_{ox} = \varepsilon_{ox}/t_{ox}$.

C_{gbx} is the gate-to-body capacitance for a device of polarity x. This capacitance is typically negligible because in strong inversion the channel shields the body from the gate.

C_{dbx} is the drain-to-body capacitance for a device of polarity x. It is given by the sum of the junction bottom and sidewall capacitances,

$$C_{dbx} = \frac{C_j AD}{\left(1 + \frac{V_{DB}}{P_B}\right)^{M_j}} + \frac{C_{jsw} PD}{\left(1 + \frac{V_{DB}}{P_{Bsw}}\right)^{M_{jsw}}}$$ (5.42)

where C_j is the capacitance per unit area of the bottom of the pn junction formed by the drain and bulk, AD is the area of the drain, V_{DB} is the drain-to-bulk voltage, P_B is the built-in potential of the junction, and M_j is the slope factor for the bottom junction. Similarly, C_{jsw} is the capacitance per unit length of the sidewall capacitance formed by the junction and the sidewall, PD is the perimeter of the drain, V_{DB} is the drain-to-bulk bias, P_{Bsw} is the built-in potential of the sidewall junction, and M_{jsw} is the slope factor for that sidewall junction. Both P_B and P_{Bsw} take the general form,

$$P_{Bx} = \frac{kT}{q} \ln\left(\frac{N_a N_d}{n_i^2}\right)$$ (5.43)

where k is Boltzmann's constant, T is temperature, q is the magnitude of the charge of an electron, N_a is the doping concentration of the substrate, N_d is the doping concentration of the junction, and n_i is the intrinsic carrier concentration of silicon at room temperature.

After substituting the expressions just presented for these capacitors and rearranging, the expression in (5.37) becomes,

$$C_{eq} = \frac{C}{2} + 2C_{GDO_n}W_n + 2C_{GDO_p}W_p + \frac{C_{GSO_n}W_n + C_{GSO_p}W_p}{2} + \frac{1}{3}C_{ox}(W_nL_n + W_pL_p)$$

$$+ \frac{(W_n + W_p)}{\pi}\left[\varepsilon_{si}\ln\left(1 + \frac{x_j}{t_{ox}}\right) + \varepsilon_{ox}\ln\left(1 + \frac{t_{gate}}{t_{ox}}\right)\right]$$

$$+ \frac{C_{j_p}AD_p}{2\left(1 + \frac{V_{DB_p}}{P_{B_p}}\right)^{M_{j_p}}} + \frac{C_{jsw_p}PD_p}{2\left(1 + \frac{V_{DB_p}}{P_{Bsw_p}}\right)^{M_{jsw_p}}} + \frac{C_{j_n}AD_n}{2\left(1 + \frac{V_{DB_n}}{P_{B_n}}\right)^{M_{j_n}}} + \frac{C_{jsw_n}PD_n}{2\left(1 + \frac{V_{DB_n}}{P_{Bsw_n}}\right)^{M_{jsw_n}}} \quad \text{(5.44)}$$

An interesting result of this analysis is that the equivalent tank capacitance is predominately bias and temperature independent. In fact, only the junction capacitors depend on bias and temperature. However, these capacitors are very small as compared to the equivalent capacitance and thus variation in these devices does not affect the frequency significantly. The remainder of the equivalent capacitance depends only on the actual tank capacitance, the geometries of the devices in the sustaining amplifier, and process geometries, none of which change over bias or temperature. The dependency on these geometric dimensions could create some concern in terms of frequency accuracy, but typically the device widths and lengths for an oscillator of this topology are quite large and thus small process changes have very little effect on the equivalent capacitance. Also, $CGDO$ and $CGSO$ depend on the source/drain junction depth and the oxide capacitance, both of which are well-controlled in modern CMOS processes since these parameters are critically related to certain process metrics such as the threshold voltage. Similarly, the junction depth, gate poly thickness, and gate oxide thickness variables within the natural log functions in (5.40) are all well-controlled. Moreover, these relationships are within a logarithmic function and thus dependence is weak. It will be shown, however, that the inductor possesses temperature dependence and this dependence dominates the temperature stability of the clock synthesizer.

From (5.44), an approximate expression for the oscillator resonant frequency can be determined from $\omega_o = (\sqrt{LC_{eq}})^{-1}$, where frequency pulling due to loss has been

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ignored. An exact expression for frequency that accounts for loss can also be determined. This loss arises from the loss in the tank in parallel with the loading of the oscillator. The sustaining amplifier presents a load of approximately $-1/G_m$, where G_m is the total transconductance given by the inverse of (5.29). Assuming that the inductor dominates the loss in the tank, and that it has an equivalent parallel loss of R_P, the total loss in the system, R, is given by the parallel combination of these two resistors or, $R_P \| -1/G_m$. Thus the frequency pulling term α, is given by $\alpha = (2RC_{eq})^{-1}$ and the modified resonant frequency is,

$$\omega_r = \sqrt{\omega^2_{\,o} - \alpha^2} \qquad (5.45)$$

Very accurate theoretical calculations of the oscillator frequency can be determined using the expression in (5.45) and the expressions just derived for ω_o and α. Also worth noting is that the oscillation frequency can be tuned by varying α, which can be achieved by simply modulating the current in the oscillator because the negative resistance presented by the amplifier varies with current. This topic will be explored further in the next section.

5.3.2.2 Tuning Range

The oscillator core can be tuned electrically using the systemic frequency pulling effect just described. Consider equation (5.45) again where $\alpha = (2RC_{eq})^{-1}$. R is equal to the parallel combination of the loss in the tank (R_P) and the loading of the amplifier (R_{amp}). R_{amp} is approximately given by $-1/G_m$. Thus, modulating the current in the oscillator core will modulate G_m, R_{amp}, R, α, and ultimately ω_r. It is useful to consider this systemic frequency pulling effect in terms of the overdesign factor, A, where $R_{amp} = R_P/A$ and thus $R = R_P/(1 - A)$. Figure 5.17 illustrates the change in frequency of a 900MHz oscillator due to varying R_{amp} and R. Additionally, the positions at which A is equal to 2, 3, and 6 are shown.

An interesting conclusion that can be drawn from Figure 5.17 is that if the overdesign factor is set to exactly one, then the actual and ideal oscillation frequencies are equal. Moreover, as the overdesign factor increases, the actual oscillation frequency is pulled further from its ideal position and the sensitivity of this pulling effect increases. Of course, the overdesign factor cannot be set to exactly one because that would provide no margin for

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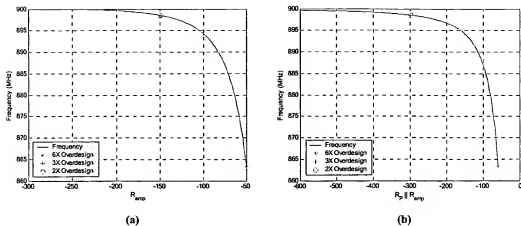
Figure 5.17 Frequency pulling effect for a 900MHz oscillator. (a) As a function of R_{amp}. (b) As a function of the total systemic loss, R.

error in the magnitude start-up criterion. Additionally, for this clock synthesis application, the overdesign factor typically lies between 2 and 6. This large overdesign factor is required in order to ensure start-up, but also in order to provide sufficient amplitude for rail-to-rail clock generation.

Tuning range can be determined as a function of the overdesign factor. First, recall that the tuning range is given by the following expression.

$$TR = \frac{\omega_{max} - \omega_{min}}{\omega_{min}} = \frac{\omega_{max}}{\omega_{min}} - 1 \tag{5.46}$$

Using the fact that at $A = 1$, $\omega_r = \omega_o$ and $R = R_P/(1-A)$ along with (5.45), an expression for ω_r can be substituted into (5.46) giving the following,

$$TR = \frac{\omega_o}{\sqrt{\omega_o^2 - \frac{(1 - A_{max})^2}{4R_P^2 C_{eq}^2}}} - 1 \tag{5.47}$$

where A_{max} is the maximum overdesign factor, which is set by the maximum current in the oscillator. The relationship to current can be determined from R_{amp}, which is selected to be $-R_P/A$. Also, $R_{amp} = -1/G_m$ and thus $A = R_P|G_m|$. To relate this expression to current, recall that $|G_m| = (g_{mn} + g_{mp})/2$ and $g_m = \sqrt{\beta I_D}$, where $\beta = 2\mu C_{ox}(W/L)$ and where μ is

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mobility, C_{ox} is the gate oxide capacitance, W and L and the transistor gate width and length respectively, and I_D is the current in each device, or one half of the tail current.

For a 900MHz oscillator with C_{eq} = 5pF, A_{max} = 5, and an inductor Q-factor of 8, corresponding to an R_P of approximately 280Ω, a tuning range of 3.4% can be achieved. Assuming that a frequency accuracy within 2% can be achieved, this tuning range is certainly adequate.

It is also worthwhile to derive a complete expression that describes the frequency tuning relationship with current. This relationship is straightforward. Begin with the frequency expression and account for frequency pulling,

$$\omega_r = \sqrt{\omega^2_o - \alpha^2} \qquad (5.48)$$

Recall that α is given by,

$$\alpha = (2RC_{eq})^{-1} \qquad (5.49)$$

R is the parallel loss in the tank and the load of the amplifier,

$$R = R_P || R_{amp} \qquad (5.50)$$

The load presented by the sustaining amplifier is given by the sum of the transconductance values for each device.

$$R_{amp} = \frac{1}{G_m} \approx \frac{-2}{g_{mn} + g_{mp}} \qquad (5.51)$$

and lastly, the current controls the transconductance in each device.

$$g_m = \sqrt{\beta I_D} \qquad (5.52)$$

The current in the tank is controlled by the bias circuitry, which will also have a certain transfer characteristic to the current in the sustaining amplifier. A complete relationship between frequency and current can be obtained by combining all of the previous expressions and simplifying,

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$$\omega_r(I_D) = \sqrt{\omega_o^2 - \cfrac{1}{\left(\cfrac{4R_P C_{eq}}{2 - R_P\left(\sqrt{2\mu_n C_{ox}\left(\frac{W}{L}\right)_n I_D} + \sqrt{2\mu_p C_{ox}\left(\frac{W}{L}\right)_p I_D}\right)}\right)^2}} \qquad (5.53)$$

where the subscripts n and p designate the device polarity. This expression will be utilized in order to graph theoretical predictions against measured and simulated data in subsequent sections.

5.3.2.3 Bias Sensitivity

The tank inductance is insensitive to bias variation and the equivalent capacitance is only weakly bias dependent through the junction capacitors C_{db}. However, the frequency pulling effect is strongly bias dependent. Recall that the load presented by the sustaining amplifier is inversely related to transconductance. Therefore, variations in the bias current through the oscillator will change the loading as well as the equivalent parallel loss and ultimately the output frequency just as described in the previous section. This relationship is inversely correlated because as the bias current decreases, the equivalent parallel loading of the amplifier increases, thus reducing α and causing ω_r to increase and approach the ideal oscillation frequency ω_o. This phenomenon can also be considered within the context of the overdesign factor, A. As current decreases, the overdesign factor is effectively decreased and thus the actual oscillation frequency approaches the ideal frequency. Consequently, the actual oscillation frequency increases with decreasing current.

A sensitivity analysis to bias can be conducted in order to determine performance. Recall the generalized sensitivity function of y to x as given by,

$$S_x^y = \frac{x \partial y}{y \partial x} \qquad (5.54)$$

The goal of this analysis is to determine the frequency sensitivity to bias variations, or $S_{I_{DD}}^{\omega_r}$, where I_{DD} is one half of the oscillator tail current. It is difficult to perform the partial differential on a complete expression that describes the relationship between I_{DD} and ω_r. Thus, it is simpler to determine this sensitivity as a product of sensitivity functions that are

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easier to derive. The resulting expression will be equivalent. Proving this, consider the sensitivity of z to x through an intermediate variable y:

$$S_x^z = S_y^z S_x^y = \left(\frac{y \partial z}{z \partial y}\right)\left(\frac{x \partial y}{y \partial x}\right) = \frac{x \partial z}{z \partial x} \tag{5.55}$$

In this analysis, the desired sensitivity will be determined from the following expression:

$$S_{I_{DD}}^{\omega_r} = S_\alpha^{\omega_r} S_R^\alpha S_{R_{amp}}^R S_{G_m}^{R_{amp}} S_{I_{DD}}^{G_m} \tag{5.56}$$

The sensitivity of ω_r is given by,

$$S_\alpha^{\omega_r} = \frac{\alpha}{\omega_r} \frac{\partial \omega_r}{\partial \alpha} = \frac{\alpha}{\omega_r} \frac{\partial}{\partial \alpha} \sqrt{\omega_o^2 - \alpha^2} = \frac{-\alpha^2}{\omega_r \sqrt{\omega_o^2 - \alpha^2}} = \frac{-\alpha^2}{\omega_r^2} = \frac{-\alpha^2}{\omega_o^2 - \alpha^2} \tag{5.57}$$

Typically α is much smaller than ω_o and thus the expression in (5.57) can be approximated by,

$$S_\alpha^{\omega_r} \approx \frac{-\alpha^2}{\omega_o^2} = \frac{-(2RC_{eq})^{-2}}{(LC_{eq})^{-1}} = \frac{-L}{4R^2 C_{eq}} \tag{5.58}$$

Next it is trivial to show that the sensitivity of α to R is -1 because the two variables are inversely related.

$$S_R^\alpha = \frac{R}{\alpha} \frac{\partial \alpha}{\partial R} = \frac{R}{\alpha} \frac{\partial}{\partial R} (2RC_{eq})^{-1} = \frac{-2RC_{eq}}{\alpha(2RC_{eq})^2} = -1 \tag{5.59}$$

The sensitivity of R to the load of the amplifier R_{amp} is determined next.

$$S_{R_{amp}}^R = \frac{R_{amp}}{R} \frac{\partial R}{\partial R_{amp}} = \frac{R_{amp}}{R} \frac{\partial}{\partial R_{amp}} \left(\frac{R_P R_{amp}}{R_P + R_{amp}}\right) \tag{5.60}$$

$$= \frac{R_{amp}}{R} \left[\frac{R_P(R_P + R_{amp}) - R_P R_{amp}}{(R_P + R_{amp})^2}\right] \tag{5.61}$$

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$$= 1 - \frac{R_{amp}}{R_P + R_{amp}} \qquad (5.62)$$

Assuming that the magnitude of the negative resistance generated by R_{amp} is $1/G_m$, where G_m is the total amplifier transconductance, the sensitivity of R_{amp} to G_m is simply -1, as was sensitivity of α to R. The transconductance loss due to the finite output impedance of the transistor can be ignored in this case because it is not a function of G_m, but rather I_{DD}.

Lastly, the sensitivity of G_m to variations in the bias current, I_{DD}, is determined. In this case, the finite output resistance of the transistor must be considered because it is dependent on the bias current. Here it is assumed that the nMOS and pMOS devices are matched and thus $G_m = -g_m$ giving,

$$S_{I_{DD}}^{G_m} = \frac{I_{DD}\partial G_m}{G_m \partial I_{DD}} = \frac{I_{DD}}{G_m}\frac{\partial}{\partial I_{DD}}\left(-g_m + \frac{1}{r_o}\right) = \frac{-I_{DD}}{G_m}\left[\frac{\partial}{\partial I_{DD}}\sqrt{\beta I_{DD}} + \frac{\partial}{\partial I_{DD}}\lambda I_{DD}\right] \quad (5.63)$$

$$= \frac{-\beta I_{DD}}{2G_m\sqrt{\beta I_{DD}}} + \lambda\frac{I_{DD}}{G_m} = \frac{-g_m}{2G_m} + \frac{1}{r_o G_m} \approx \frac{1}{2} \qquad (5.64)$$

where $\beta = 2\mu C_{ox}(W/L)$, r_o is the transistor output resistance, and λ is the channel length modulation factor. The approximation in (5.64) is based on the fact that the second term is very small relative to 1/2 because r_o is large.

Finally, a complete expression for the sensitivity of the oscillation frequency to bias variations can be determined by the product of the derived sensitivities:

$$S_{I_{DD}}^{\omega_r} = S_\alpha^{\omega_r}S_R^\alpha S_{R_{amp}}^R S_{G_m}^{R_{amp}}S_{I_{DD}}^{G_m} = -\frac{L}{8R^2 C_{eq}}\left(1 - \frac{R_{amp}}{R_P + R_{amp}}\right) \qquad (5.65)$$

The output resistance of the amplifier is designed such that $R_{amp} = -R_P/A$, where A is the overdesign factor. Using this fact, and substituting, the following is obtained.

$$S_{I_{DD}}^{\omega_r} = -\frac{L}{8\left(\dfrac{R_P}{1-A}\right)^2 C_{eq}}\left(1 - \frac{1}{1-A}\right) \qquad (5.66)$$

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At this point, an estimate of the bias sensitivity for a practical oscillator is considered. For a 900MHz oscillator assume that $L = 6.25$nH, $C_{eq} = 5$pF, $A = 4$, and the inductor Q-factor is 8, corresponding to an R_P of approximately 280Ω. Evaluating (5.66) with these variables yields a sensitivity of 2.4%.

Although high sensitivity is desirable for tuning, frequency sensitivity due to power supply variations or noise is highly undesirable. Unfortunately, the expression in (5.66) presents very little insight into how the sensitivity can be improved. The largest dependency is on R_P. As R_P increases, the sensitivity is reduced as would be expected because a larger R_P corresponds to a less lossy inductor. Of course, realizing the least lossy inductor possible is already a design objective based upon short-term stability considerations. The overdesign factor, A, is typically set based upon amplitude considerations, thus leaving only the ratio of L and C_{eq}. However, for a fixed oscillation frequency, this ratio cannot change.

The solution to this problem is actually quite simple. The current reference can be designed to be power supply independent. Consider that variations in I_{DD} arise only from variations in the power supply, V_{DD}. Thus, a complete expression for bias sensitivity is given by $S_{V_{DD}}^{\omega_r} = S_{I_{DD}}^{\omega_r} S_{V_{DD}}^{I_{DD}}$. A band-gap reference can provide a constant current over bias with a sensitivity of less than 1%. Using such a bias, reduces the frequency sensitivity to bias to less than 0.024% for the example given previously.

Lastly, it is useful to derive a complete expression that describes frequency as a function of voltage. Such an expression is relatively simple to derive. The expression in (5.53) shows the relationship between one half of the tank tail current and frequency. This expression simply requires extension in order to determine the relationship between current and the power rail, which would be of the following form,

$$\omega_r(V_{DD}) = \sqrt{\omega_o^2 - \frac{1}{\left(\frac{4R_P C_{eq}}{2 - R_P(\sqrt{\beta_n I_D(V_{DD})} + \sqrt{\beta_p I_D(V_{DD})})}\right)^2}} \quad (5.67)$$

where $I_D(V_{DD})$ will be presented with the bias circuit in a subsequent section.

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5.3.2.4 Temperature Coefficient

The temperature sensitivity can also be predicted by determining a sensitivity function for temperature. This sensitivity can be complicated to analyze because variation is due to several factors. First, the bias current varies due to the temperature coefficient of the biasing resistor and due to variation in the threshold voltage and the mobility of the active devices. Second, the transconductance of the amplifier changes due to changes in mobility over temperature. Third, the junction capacitors vary with temperature. Fourth, the Q-factor of the inductor decreases over temperature and thus the frequency pulling is changed. Fifth, the inductance changes with temperature. Of all of these variations, the dominating factor is the change in inductance over temperature. However, the current variation due to the biasing resistor also contributes to the temperature coefficient. One may wonder if the temperature variation of the junction capacitors is significant because a clear relationship between capacitance and temperature has been shown. Although strong temperature dependence exists, the magnitude of the tank capacitance is much larger than the magnitude of the junction capacitors. Thus, the variation in these devices is insignificant.

Because each of the aforementioned factors are independent, two sensitivity functions can be derived and added together.

$$S_T^{\omega_r} = S_{\omega_o}^{\omega_r} S_L^{\omega_o} S_T^L + S_{I_{DD}}^{\omega_r} S_T^{I_{DD}} \tag{5.68}$$

where all terms are as defined previously. In the last section, $S_{I_{DD}}^{\omega_r}$ was derived. $S_T^{I_{DD}}$ is dependent on the biasing circuit and will be shown later. Thus, only the first product in (5.68) requires derivation, which is determined next.

$$S_{\omega_o}^{\omega_r} = \frac{\omega_o \partial \omega_r}{\omega_r \partial \omega_o} = \frac{\omega_o}{\omega_r} \frac{\partial}{\partial \omega_o} \sqrt{\omega_o^2 - \alpha^2} \approx \frac{\omega_o \partial \omega_o}{\omega_r \partial \omega_o} = \frac{\omega_o}{\omega_r} \approx 1 \tag{5.69}$$

where the approximation $\omega_r = \omega_o$ has been made. Next, the sensitivity of ω_o to L is determined.

$$S_L^{\omega_o} = \frac{L}{\omega_o} \frac{\partial \omega_o}{\partial L} = \frac{L}{\omega_o} \frac{\partial (LC_{eq})^{-1/2}}{\partial L} = -\frac{1}{2} \frac{L}{\omega_o} (LC_{eq})^{-3/2} C_{eq} = -\frac{1}{2} \tag{5.70}$$

Inductance variation over temperature can be estimated by a linear model of the following form,

$$L = L_o[1 + TC_1(T - T_{nom})]$$ (5.71)

where L_o is the nominal inductance at T_{nom} (in Kelvin) and TC_1 is the linear temperature coefficient. Solving for the temperature sensitivity gives the following,

$$S_T^L = \frac{T}{L}\frac{\partial L}{\partial T} = \frac{T}{L}\frac{\partial}{\partial T}L_o[1 + TC_1(T - T_{nom})] = \frac{TL_oTC_1}{L} = T(TC_1)$$ (5.72)

where in the final reduction, $L = L_o$. Substituting into (5.68) gives,

$$S_T^{\omega_r} = \frac{-T(TC_1)}{2} + S_{I_{DD}}^{\omega_r}S_T^{I_{DD}}$$ (5.73)

Recall that $S_{I_{DD}}^{\omega_r}$ is negative and it will be shown that $S_T^{I_{DD}}$ is also negative. Thus, the first term has a negative sensitivity to temperature and the second term has a positive sensitivity to temperature. This provides an obvious compensation technique. Specifically, the current can be modulated over temperature in order to offset frequency variation due to the inductor.

Typically, temperature sensitivity is specified in terms of a fractional temperature coefficient, as defined by,

$$TC_{\omega_r} = \frac{1}{\omega_r}\frac{\partial \omega_r}{\partial T} = \frac{S_T^{\omega_r}}{T}$$ (5.74)

and often this measure is expressed in units of part per million as given by,

$$TC_{\omega_r,ppm} = \frac{1}{\omega_r/10^6}\frac{\partial \omega_r}{\partial T} = 10^6 TC_{\omega_r}$$ (5.75)

Again it is worth considering the sensitivity for a typical case. The parameters presented previously for a 900MHz oscillator include C_{eq}=5pF and $S_{I_{DD}}^{\omega_r} = -0.024$. Typical values

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for the remaining parameters are $S_T^{I_{DD}} = -0.04$, and $TC_1 = 3 \times 10^{-4}$. With these values, $TC_{\omega r, ppm} = -81 ppm/°C$.

Lastly, a complete expression that describes frequency as a function of temperature can be determined using (5.53),

$$\omega_r(T) = \sqrt{\frac{1}{L(T)C_{eq}} - \frac{1}{\left(\frac{4R_P C_{eq}}{2 - R_P(\sqrt{\beta_n I_D(T)} + \sqrt{\beta_p I_D(T)})}\right)^2}} \qquad (5.76)$$

where $L(T)$ is given by (5.71), and $I_D(T)$ will be shown with the bias circuitry in a subsequent section.

5.3.3 Signal Characteristic Analysis

If the nMOS and pMOS transistors are matched such that all four devices have the same output resistance and the same transconductance, then the waveform will have a 50% duty cycle. Of course some variation from this ideal is expected due to process variation.

The amplitude of the signal across the tank can be determined by considering the case where all of the tail current, I_{tail}, is switched through the tank. Recall that by the definition of resonance given in Chapter II, the admittance of the inductor and capacitor will cancel. Thus, the tank presents only a resistance, R_P, to the current passing through it. The product of this current and the equivalent tank resistance determines the amplitude of the signal as given by,

$$V_{max} = I_{tail}R_P \qquad (5.77)$$

R_P can be determined by a transformation from the component Q of each device. The component Q, sometimes referred to as the series Q or Q_s, is defined by $Q_s = Im(Z)/Re(Z)$ where the Z is the complex impedance across the 2-ports of the device as shown in Figure 5.18a. For the parallel case, shown in Figure 5.18b, the Q, or Q_p, is defined by $Q_p = Re(Z)/Im(Z)$. A transformation between the series and parallel rep-

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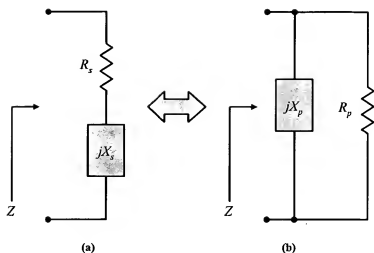
Figure 5.18 Series to parallel transformation of component Q. (a) Series network. (b) Equivalent parallel network.

resentations can be determined simply from these definitions. It is trivial to show that the parallel resistor, R_p, can be determined from R_s by,

$$R_p = R_s(1 + Q^2) \qquad (5.78)$$

Now, assuming that the varactor has a real series loss, R_c, and quality-factor Q_c, and the inductor has a real series loss, R_L, and quality factor, Q_L, the equivalent parallel tank resistance can be determined from,

$$R_P = R_c(1 + Q_c^2) \big|\big| R_L(1 + Q_L^2) \qquad (5.79)$$

For even moderate values of Q, the expression in (5.79) can be simplified by dropping the 1 within each parentheses. Moreover, for large capacitor Q, the equivalent parallel resistance can be approximated by the equivalent resistance of the inductor alone. Thus, (5.77) can be approximated by,

$$V_{max} \approx I_{tail} Q_L^2 R_L = I_{tail} Q_L \omega L \qquad (5.80)$$

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5.3.4 Detailed Noise and Short-Term Frequency Stability Analysis

Noise in the oscillator gives rise to short-term frequency instability, which is highly undesirable for a clock signal. A detailed analysis is presented next in an effort to determine the contributing factors to this noise. Several phase noise analysis approaches have been presented in Chapter II, the most useful of which is the linear time-varying model presented by Hajimiri and Lee [14]. The oscillator utilized in this work will be analyzed with this approach as shown in [107].

In [14] and in Chapter II it was shown that the phase noise of an oscillator can be determined from the linear time-variant impulse response of the system, $h_\phi(t,\tau)$, and the input noise current, $i(\tau)$, or specifically,

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau) i(\tau) d\tau \tag{5.81}$$

In [14] it was shown that, $h_\phi(t,\tau)$, can be represented by an impulse sensitivity function or ISF. As shown in Chapter II and [14], (5.81) becomes,

$$\phi(t) = \int_{-\infty}^{t} \frac{\Gamma(\omega_o \tau)}{q_{max}} i(\tau) d\tau \tag{5.82}$$

where $\Gamma(\omega_o t)$ is the ISF and q_{max} is the maximum charge injection into the tank. The latter term can be determined from the maximum voltage amplitude, derived in (5.77), where $q_{max} = C_{eq} V_{max}$ and C_{eq} is the equivalent tank capacitance.

The expression in (5.82) can be further simplified for specialized cases. Consider only white noise sources such that $i(\tau)$ has a constant PSD given by $\overline{i_n^2}/\Delta f$, which is independent of τ. Also, for the selected topology the ISF is nearly a sinusoid because the current injected into the tank is also nearly sinusoidal and the tank suppresses harmonics of the fundamental frequency. With these assumptions, the integral in (5.82) can be evaluated. Using (2.40), as shown in Chapter II, the result is,

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$$\left(\frac{N_o}{P_o}\right)_{f_m} = \frac{\Gamma_{rms}^2 \; \overline{i_n^2}/\Delta f}{4\pi^2 f_m^2 \; q_{max}^2} \tag{5.83}$$

where Γ_{rms} is $1/\sqrt{2}$ because again, $\Gamma(\omega_o t)$ is nearly sinusoidal. Recall that the ISF is a dimensionless function with unity amplitude. The remaining challenge in this analysis is to determine $\overline{i_n^2}/\Delta f$. In fact, this is nontrivial because the noise injected into the tank changes throughout each oscillation cycle. For some portions of the cycle, a transistor may be in the linear region of operation while in others it may be saturated. The simplest approach to dealing with this fact is to analyze the worst case, which is when all four transistors are saturated and on, corresponding to the balanced, or differential zero-crossing, state. To select this operational point for analysis is also rather intuitive. Consider that the ISF is maximum at the signal zero-crossing because noise injected at this point possess the greatest potential for inducing phase noise.

The complementary cross-coupled pair is shown in Figure 5.19a with all noise sources. Each transistor contributes a noise current and the inductor contributes noise due to the finite resistance across the device. The schematic in Figure 5.19a can be transformed to the differential small-signal equivalent circuit shown in Figure 5.19b, where r is the parallel combination of the pMOS and nMOS output resistances. The currents, i_1 and i_2, represent the current in the left and right legs of the circuit respectively. The tail current presents an output resistance which can be ignored because it is applied at a common mode point. The schematic in Figure 5.19b can be transformed into the schematic in Figure 5.19c by replacing the current source and resistor pair in Figure 5.19b with a Thévenin equivalent source and simplifying. At resonance, the resistance, $2r$, is cancelled by the negative resistance generated by the amplifier. From this simplified circuit, the total noise power from the transistors can be determined by adding the square magnitude of each uncorrelated noise source. The noise currents i_1 and i_2 are each the sum of the nMOS and pMOS noise sources. Thus, the total noise power from the amplifier is given by,

$$\overline{i_{amp}^2} = \frac{\overline{i_2^2}}{4} + \frac{\overline{i_1^2}}{4} = \frac{1}{4}(\overline{i_n^2} + \overline{i_p^2} + \overline{i_n^2} + \overline{i_p^2}) = \frac{1}{2}(\overline{i_n^2} + \overline{i_p^2}) \tag{5.84}$$

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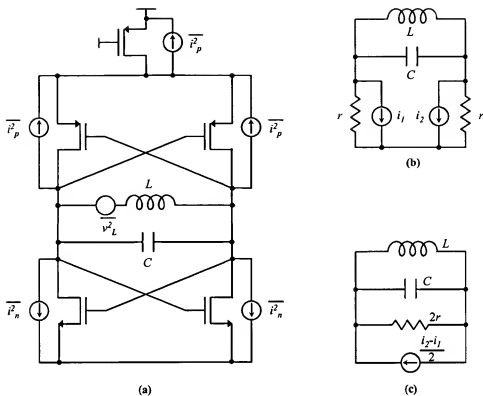
Figure 5.19 Noise analysis schematics for the complementary cross-coupled oscillator. (a) Transistor schematic indicating all noise sources. (b) Equivalent differential small-signal schematic. (c) Reduced small-signal schematic after transformation [107].

Each noise density, i_x where x is either n or p, is given by,

$$\frac{\overline{i_x^2}}{\Delta f} = 4kT\gamma\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)$$
(5.85)

where k is Boltzman's constant, T is temperature, γ is a constant between 2 and 3 for short channel devices [108], μ is the device mobility, C_{ox} is the oxide capacitance per unit area, W is the transistor width, L is the transistor length, V_{GS} is the gate to source voltage, and V_T is the threshold voltage. Lastly, the noise contribution from the inductor must be determined. The noise source, $\overline{v_L^2}$, is due to the series ohmic loss, R_s, in the inductor and thus,

$$\frac{\overline{v_L^2}}{\Delta f} = 4kTR_s$$
(5.86)

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The noise voltage in (5.86) can be converted to a parallel current across the tank given by,

$$\frac{\overline{i_L^2}}{\Delta f} = 4kT\frac{R_s C_{eq}}{L} \tag{5.87}$$

Now, (5.83) can be evaluated using (5.80), (5.84), and (5.87) giving,

$$\left(\frac{N_o}{P_o}\right)_{f_m} = 10\log\left(\frac{\Gamma_{rms}^2 \; \overline{i_n^2}/\Delta f}{4\pi^2 f_m^2 \; q_{max}^2}\right) = 10\log\left(\frac{\overline{i_L^2}/\Delta f + \overline{i_{amp}^2}/\Delta f}{8\pi^2 f_m^2 (C_{eq} I_{tail} Q\omega L)^2}\right) \tag{5.88}$$

and thus the phase noise can be determined for an arbitrary offset, f_m. Once obtained, the phase noise can be converted to jitter with the expressions derived in Chapter II.

Flicker noise has been ignored in this analysis and yet it contributes significantly to the total phase noise of the oscillator. The primary contribution comes from the tail device where low frequency noise is upconverted to the fundamental frequency as shown in [89]. Waveform symmetry has been shown to reduce this upconversion. Correspondingly, in [14], it was shown that the DC value of the ISF determines the amount of flicker noise upconversion. Ideally, the selected topology provides perfect waveform symmetry and thus the DC value of the ISF is zero. However, due to device mismatch, this is not the case. Rather than analyze the effects of device mismatch, it more instructive to investigate techniques by which flicker noise injection into the tank can be reduced. This is the topic of the next section.

5.3.5 Noise Mitigation Techniques

In this section, several noise mitigation techniques are described and examined for the complementary cross-coupled oscillator topology. In Chapter IV, this topology was selected based upon results from systemic analysis of the oscillator from which topological aspects that affect the phase noise performance could be predicted. In contrast, the techniques presented here are based upon considering the aspects of device physics that contribute to the phase noise.

5.3.5.1 Reducing Flicker Noise Upconversion

In this section, three approaches for reducing flicker noise upconversion are described for the complementary cross-coupled oscillator. The techniques considered here include:

- pMOS vs. nMOS Tail Current Source

  pMOS devices exhibit a flicker noise power spectral density that is as much as 10 times less than comparable nMOS devices [89], which is due to the fact that pMOS devices are typically buried channel devices in modern CMOS processes. Thus, a charge carrier in a pMOS device is less exposed to the oxide interface where energy trapping states exist. It can be predicted that the device polarity change will realize gains of approximately 10dB in terms of phase noise performance.

- Filtering the Flicker Noise

  In [109], a noise filtering technique around the tail current has been presented. This technique provides good performance but requires an additional capacitor and inductor in order to bias the oscillator. Experimental results indicate that the phase noise PSD can be improved by up to 7dB with this technique [109].

- Weak Inversion Tail Current Source

  By placing the tail current source device on the edge of weak inversion, as opposed to strong inversion, flicker noise is reduced. Previous work has shown flicker noise power to be a function of gate voltage, where the input-referred noise power decreases with decreasing gate voltage [110]. This is likely related to an increase in gate oxide trap density with increased gate voltage. Consider that as the gate voltage is increased, more trapping states are exposed to the charge carriers in the channel.

Of these options, only the first is practical for this application, as it involves merely a change in the tail current device polarity. The second option requires an additional capacitor and inductor, the latter of which substantially increases the total size of the clock syn-
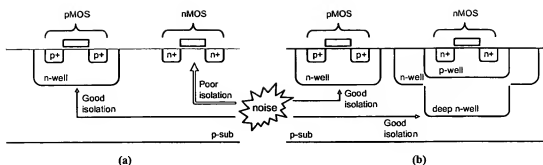
Figure 5.20 Illustration of the deep *n*-well process option. (a) Poor nMOS device isolation from the substrate exists for the standard *n*-well process. pMOS devices are well isolated. (b) The deep *n*-well option isolates the nMOS device in its own p-well.

thesis block, making it inappropriate for this work. The third option, though interesting, would cause the device sizes to become prohibitively large in order to force the tail transistor into weak inversion at high current. For some applications, this may be an option where large signal amplitude, and thus high current, is not required.

5.3.5.2 Device Isolation

The *TSMC* process, like most modern CMOS processes, is an *n*-well process. This creates isolation problems for the nMOS device since all nMOS devices share a common substrate. Thus noise can easily couple into the nMOS device and potentially corrupt the oscillator signal as shown in Figure 5.20a. The pMOS devices do not suffer from this problem because they are isolated within the *n*-well. Fortunately, the MM/RF process has a deep *n*-well option that allows the nMOS device to be fabricated in its own *p*-well as illustrated in Figure 5.20b. The entire oscillator core will be designed using the deep *n*-well option such that all nMOS and pMOS devices are isolated from the substrate.

5.4 System Architecture

Although the oscillator is certainly the most important circuit in the clock synthesizer, several supporting circuits are required in order to generate the clock signal. First, in order to ensure that the signal is nearly rail-to-rail, the signal from the oscillator is amplified by a wide-band RF amplifier, pictured in Figure 5.21a. Then the signal is fed into a flip-flop frequency divider chain which also squares the signal. The flip-flop frequency divider is differential and positive-edge triggered. Frequency division is achieved by clocking the flip-

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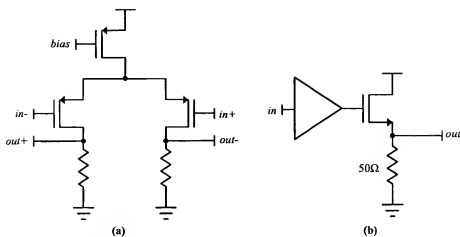
Figure 5.21 Supporting system circuits. (a) Wide-band RF amplifier. (b) 50Ω output stage.

flop with the reference signal and feeding the complementary output back onto the D-input. Thus, for every complete period of the clock signal, the state of the flip-flop changes once, corresponding to half of the output period. Each output signal is buffered and then driven off-chip with a 50Ω output driver, shown in Figure 5.21b, in order to accommodate the instrumentation. In an embedded application, these drivers would not be required and the clock signal could simply be buffered off of the frequency divider chain and to the processor.

The entire clock synthesis system is shown schematically in Figure 5.22. With this architecture, frequencies of the form $f_o/2^n$ are synthesized, where n is a positive integer.
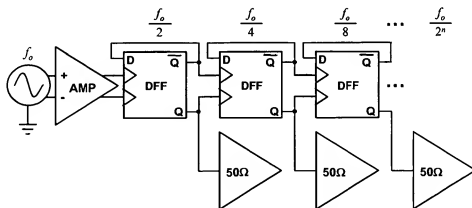
Figure 5.22 Architecture of the monolithic and top-down clock synthesizer with micromachined RF reference.

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Certainly, more elaborate frequency synthesis approaches could be developed that would accommodate a broader range of frequencies, the most interesting of which is fractional frequency synthesis. Techniques such as phase switching [111], could be explored in the future in order to achieve such a goal.

5.5 Detailed Design

The previous sections provided useful analytical formulations for design and comparison to measured results from prototyped devices. In this section, the detailed design for the 900MHz monolithic and top-down clock synthesis system is presented. Results from many of the previous section are utilized in this design effort.

5.5.1 Complementary Cross-Coupled *LC* Oscillator

5.5.1.1 Oscillator

A design procedure has been developed for the oscillator that draws upon the analytical results derived previously. It is presented next.

- Begin by considering that the variable that affects the phase noise performance of the oscillator the most significantly is the Q-factor of the tank. Directly related to the Q-factor is the parallel loss, R_P. This parallel loss is dominated by the parallel loss in the inductor, which is given by,

$$R_p = R_s(1 + Q^2) \approx Q^2 R_s \qquad (5.89)$$

where $Q = \omega L / R_s$. With the substitution $R_s = \omega L / Q$, $R_p \approx Q\omega L$ and thus increasing L increases R_P. Increases in L cause corresponding increases in R_s and thus Q remains approximately constant [3]. The only disadvantage is that as L increases, the self-resonant frequency decreases because the parallel capacitance increases with area. Thus, the first design objective is to determine the largest acceptable L with these factors considered. In this work, L was selected to be 6nH.

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- With L determined, the parallel loss can be estimated by assuming a Q-factor of 8 based on previously measured results. Using $R_p \approx Q\omega L$, R_P is 270Ω at 900MHz.

- Next, the maximum voltage amplitude should be set to correspond to an operation point on the edge of the voltage-limited regime. For the given biasing scheme, the gate of the current source transistor that feeds the tank will be very near ground. Thus, the corresponding V_{GS} will be approximately V_{DD}. In order for the tail current device to remain saturated, a drain to source voltage of V_{DD}-V_T must be maintained and this voltage corresponds to the maximum voltage that the tank can achieve. Therefore, the required tail current is given by,

$$I_{tail} = \frac{V_{DD} - V_T}{R_P} \qquad (5.90)$$

  where V_{DD} = 1.8V and V_T = 450mV, giving I_{tail} = 5mA.

- Next, the required transconductance of the sustaining amplifier is determined. The start-up condition is given by $G_m > 1/R_P$ and thus typically the transconductance is set such that $G_m = A/R_P$ where A is the over-design factor. For this design, an overdesign factor of 6 was selected, thus requiring a transconductance of approximately 22.2mS.

- The total transconductance of the amplifier is given by $G_m = (g_{m_n} + g_{m_p})/2$. The transconductance values for the nMOS and pMOS devices vary due to differences in the mobility for each device. The individual device transconductance is given by $g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_D}$. Thus the expression for the system transconductance can be rewritten in terms of only the nMOS device geometry as follows,

$$G_m = \frac{g_{m_n} + \sqrt{\frac{\kappa}{\mu_n/\mu_p}} g_{m_n}}{2} \qquad (5.91)$$

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where κ is the ratio of the aspect ratios between the pMOS and nMOS devices. For this work, the ratio was selected to be 1.5 in order to limit the size of the pMOS devices to a reasonable value. The ratio of the device mobilities is 4.5. Using these values, the required nMOS transconductance can be found from $g_{m_n} = 2G_m/(1 + \sqrt{\kappa \mu_p/\mu_n})$. which yields 28.2mS. Finally, the geometry for the nMOS device can be determined as shown next.

$$\left(\frac{W}{L}\right)_n = \frac{g_{m_n}^2}{2\mu_n C_{ox} I_D} \qquad (5.92)$$

Substituting I_D = 5mA, μ_n = 0.026 cm²/V-s, and C_{ox} = 8.46mF/m gives 361. This result was rounded to an aspect ratio of 400.

- Next, a reasonable gate length was selected such that the aspect ratio does not cause the devices to be unreasonably wide. However, a longer channel length is preferred because the output resistance will be increased and thus the total transconductance will not be reduced. Here, a length of 0.25µm was selected which yields an nMOS device length of 100µm and a pMOS device length of 150µm.

- With the devices geometries determined, the tank capacitance can be solved. The oscillation frequency, including frequency pulling, is given by the following expression.

$$\omega_r = \sqrt{\omega_o^2 - \alpha^2} \qquad (5.93)$$

After substituting expressions for ω_o and α, the following quadratic equation in C_{eq} is obtained.

$$0 = C_{eq}^2(\omega_r^2) + \left(-\frac{1}{L}\right)C_{eq} + \frac{1}{4R^2} \qquad (5.94)$$

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The loss, R, is given by the parallel combination of the sustaining amplifier and the loss in the tank, or $R = Q\omega_r L \parallel (-1/G_m)$. The solution to (5.94) has two roots, the correct one of which is 4.64pF for this design. Referring to (5.37), the total equivalent capacitance is given by the following.

$$C_{eq} = 2C_p + \frac{C}{2} + \frac{C_D}{2} \tag{5.95}$$

The capacitors C_p and C_D can be determined using the geometries derived in the step prior to this one and the expressions in (5.38) and (5.44). After substitution into (5.95), C is found to be 8.3pF.

5.5.1.2 Current Bias

A simple current reference circuit, pictured in Figure 5.23, was designed in order to enable easy control of the current entering the oscillator. The port labeled V_{ctrl} is typically ground, but the voltage can be varied in order to adjust the current in the tank. This approach was taken in to order determine the achieveable tuning range by frequency pulling via current modulation. However, this design decision comes with some disadvantages including the fact that the bias current is very sensitive to power supply variations. Here, an expression for the nominal current is derived as is the power supply and temperature sensitivity.
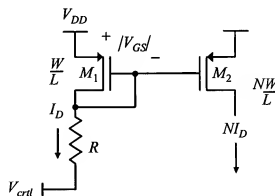
Figure 5.23 Simple current mirror bias allowing the tank current to be modulated easily with the control voltage V_{ctrl}.

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The current in the oscillator tank is set by the current in M_1 as shown in Figure 5.23. The device M_2 is scaled to be N-times larger than M_1 and thus the current through M_2 is approximately N times larger than that current through M_1. Using the long channel MOSFET current expression, the following can be determined,

$$I_D = \beta'(V_{GS} - V_T)^2 = \beta'(V_{DD} - I_D R - V_T)^2 \qquad (5.96)$$

where $\beta' = \mu C_{ox} W / 2L$. Rearranging (5.96) leads to a quadratic expression in R given by,

$$0 = R^2(\beta' I_D^2) + R(2\beta' I_D V_T - 2\beta' V_{DD} I_D) + (\beta' V_{DD}^2 - 2\beta' V_{DD} V_T + \beta' V_T^2 - I_D) \qquad (5.97)$$

and thus (5.97) can be solved for an arbitrary R given the desired current, the power supply, and the device properties. For this design $I_D = 3\text{mA}$, $\beta' = 2.2 \times 10^{-3}$, from $L_1 = 0.4\mu\text{m}$, $W_1 = 36\mu\text{m}$, $\mu_p = 0.0058\text{cm}^2/\text{V-s}$, and $C_{ox} = 8.46\text{mF}/\mu\text{m}^2$, which determines that $R = 60\Omega$. After simulation of this current reference, the resistor was modified to 50Ω due to second order effects that were not considered in this analysis.

Next, a power supply sensitivity function can be determined for this bias topology.

$$S_{V_{DD}}^{I_D} = \frac{V_{DD}}{I_D}\frac{\partial I_D}{\partial V_{DD}} = \frac{V_{DD}}{I_D}\frac{\partial}{\partial V_{DD}}[\beta'(V_{DD} - I_D R - V_T)^2] \approx \frac{V_{DD}}{I_D}\frac{\partial}{\partial V_{DD}}[\beta'(V_{DD} - V_T)^2]$$

$$= \frac{V_{DD}}{I_D}2\beta'(V_{DD} - V_T) = \frac{2V_{DD} I_D}{I_D(V_{DD} - V_T)} = \frac{2V_{DD}}{(V_{DD} - V_T)} \qquad (5.98)$$

Lastly, the temperature sensitivity can be determined from the following.

$$S_T^{I_D} = S_R^{I_D} S_T^R \qquad (5.99)$$

Using (5.96), $S_R^{I_D}$ can be determined,

$$S_R^{I_D} = \frac{R}{I_D}\frac{\partial I_D}{\partial R} = \frac{R}{I_D}\frac{\partial}{\partial V_{DD}}[\beta'(V_{DD} - I_D R - V_T)^2] = R\beta(2I_D + 2V_T - 2V_{DD}) \qquad (5.100)$$

Resistors are modelled in *SPICE* by a simple quadratic equation,

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$$R = R_o[1 + TC_1(T - T_{nom}) + TC_2(T - T_{nom})^2] \tag{5.101}$$

where R_o is the nominal resistance at T_{nom} and TC_1 and TC_2 are temperature coefficients. Because the change in resistance is nearly linear over temperature, (5.101) can be simplified to account for only the linear temperature coefficient, thus giving the following sensitivity,

$$S_T^R = \frac{T}{R}\frac{\partial R}{\partial T} = \frac{T}{R}\frac{\partial}{\partial T}R_o[1 + TC_1(T - T_{nom})] = \frac{TR_oTC_1}{R} = T(TC_1) \tag{5.102}$$

where in the final reduction, $R = R_o$. Thus,

$$S_T^{I_D} = R\beta(2I_D + 2V_T - 2V_{DD})T(TC_1) \tag{5.103}$$

Both of these sensitivity expressions will be used to compare theoretical predictions with measured results.

Lastly, in order to use the expressions in (5.67) and (5.76), $I_D(V_{DD})$ and $I_D(T)$ must be determined. From (5.96), the first expression can be approximated by the following.

$$I_D(V_{DD}) \approx \beta'(V_{DD} - V_T)^2 \tag{5.104}$$

Similarly, $I_D(T)$ can be determined from,

$$I_D(T) = \frac{V_{DD} - |V_{GS}|}{R(T)} \tag{5.105}$$

where $R(T)$ is given by (5.101). Use of (5.104) and (5.105) in (5.67) and (5.76) requires scaling by N, as shown in Figure 5.23, and division by 2 for each leg of the sustaining amplifier. For this design $N = 1.8$, giving a tank current near 5mA.

5.5.2 Reference

Based upon the design presented in the previous sections, an inductor of 6nH and a capacitor of 8.3pF is required. The capacitance was realized using a 3-by-3 MiM structure of 8.3pF on each side and a unit capacitance of 922fF. This structure was developed to support

Design parameter	Value
Target inductance (L)	6nH
Theoretical inductance (L)	5.60nH
Empirical inductance (L)	6.04nH
Topology	Square hollow-core
Frequency (f_o)	900MHz
Resistivity (ρ)	28.3nΩ-m
Skin depth at f_o (δ)	2.82μm
Dielectric permittivity (ε_{ox})	1
Fitting parameter (C_{sub})	10^{-14}fF/m^2
Fitting parameter (R_{sub})	$10^{-5}\Omega$/m^2
Series loss (R_s)	4.04Ω
Interwire coupling (C_s)	5.97fF
Substrate coupling (C_{ox})	27.8fF
Substrate capacitance (C_{si})	2.56×10^{-22}F
Ohmic loss (R_{si})	391Ω
Trench overhang	50μm
Length (L)	3410μm
Relative permeability (μ_r)	~1
Number of turns (n)	4.5
Mean radius (a)	96.125μm
Radius (r)	132.75μm
Hollow core radius (R)	60μm
Thickness (t)	2μm
Width (w)	15μm
Turn spacing (s)	1.5μm
Device material	Al
Calculated Q-factor at f_o (Q)	8.38

Table 5.4 Inductor design parameters for the clock synthesizer.

the release etch in the event that one is developed at a later date. The components were designed in a manner identical to that presented previously and here only a summary of the inductor design is presented in Table 5.4 on the previous page. The most notable modification from the previous work is the increased trench overhang, which was increased based upon the measured results from the reference design section of this dissertation.

It is worth noting that the total tank capacitance can be reduced by one quarter if tuning by frequency pulling is the only technique employed. In fact, this is another significant benefit to the frequency pulling approach. With varactor tuning, two equal and identical varactor arrays are required, although only half of each of these capacitors actually contribute to C_{eq} as shown in (5.37). This is because the two varactor arrays are split by the tuning voltage, which is applied to the center of the tank as shown in Figure 5.15a. In future versions of this work, it is likely most appropriate to replace the two varactor arrays with one MiM capacitor array that is placed across the tank. Doing so greatly reduces the total area required for the tank capacitance.

5.5.3 System

5.5.3.1 Amplifier

The amplifier is included in order to provide level shifting to the midpoint of the flip-flop switching cycle and in order to maximize the signal swing. Moreover, this amplifier serves the purpose of decreasing the rise and fall times of the oscillator signal by increasing the slew rate. The design procedure for this stage is straightforward and outlined next.

- Begin by selecting a low bias current. For this design, the bias is selected to be 2mA (1mA/side). Achieve the desired level-shifted output at this current using $V_{out_{DC}} = I_{bias}R$. The switching midpoint for the divider circuits is at approximately 1V, thus R should be 1kΩ on each side of the amplifier.

- The magnitude of the gain for this stage is approximately $g_m R$. Choose an appropriate gain in order to square the wave and increase the rise and fall times of the signal. For this design, a gain of 8 was selected. Now determine the required device geometry from g_m using the fact that

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$g_m = A_v/R$ and $\sqrt{2\mu C_{ox}(W/L)I_D} = A_v/R$ and   therefore $\frac{W}{L} = (A_v/R)^2/(2\mu C_{ox}I_D)$. Substituting all variables gives $W/L=146$. Choosing the minimum device length, $L=0.18\mu m$, gives $W=25\mu m$, when rounded to the nearest $5\mu m$.

- Lastly, confirm the bandwidth. The bandwidth dominated by C_{gd} for each device and is approximately given by $BW \approx 2\pi/(2C_{gd}R)$ where $C_{gd}=CGD0W$. For this design, the bandwidth is approximately 9GHz, which is sufficient, as it is one order of magnitude above the operation frequency of this oscillator.

5.5.3.2 Frequency Dividers

The frequency division circuits are simple D flip-flops with feedback as shown in Figure 5.24. The transistor-level implementation of each gate is shown in Figure 5.25 on the following page.

5.5.3.3 Output Drivers

The output drivers were designed to accommodate the 50Ω test equipment. Unfortunately, due to size constraints with prototype runs through *TSMC*, the output drivers could not be sized to swing rail-to-rail. Thus, the drivers were designed to source 2mA into 50Ω on-chip
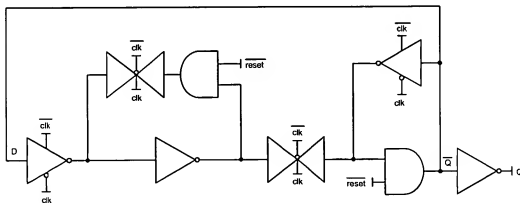
Figure 5.24   Differential input D flip-flop positive-edge triggered frequency divider circuit with Q output fed back onto the D input. The circuit achieves frequency division by a factor of two.
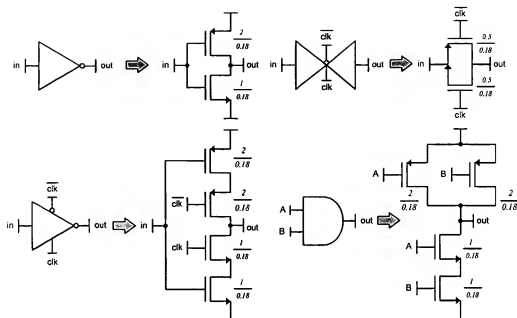
Figure 5.25   Transistor-level implementation of the gates comprising the _D_ flip-flop frequency divider.

in parallel with the 50Ω instrumentation, giving a 50mV amplitude at the test instrumentation. The designed output driver can easily drive several GHz into a load of several pF.

5.6 Analytical and Simulation Results

Simulations take into account several second order effects that were not considered in the analysis presented in the previous sections. As such, some design parameters were modified in order to achieve a target frequency near 900MHz. Modifications to note include the fact that the actual tank current was 5.42mA, as opposed to 5mA and the RF amplifier current was 1.74mA (0.87mA/side) as opposed to 2mA (1mA/side). The simulated oscillation frequency is 897MHz. Lastly, the overdesign factor is closer to 4. In the following sections, the results from simulation are presented.

5.6.1 DC conditions

Table 5.5 summarizes the simulated DC conditions for the clock synthesis system.

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Variable	Value
Power rail (V_{DD})	1.80V
Reference current (I_{ref})	3.00mA
Tank current (I_{tank})	5.42mA
Amplifier current (I_{amp})	1.74mA
Total RMS current (I_{total})	9.34mA
Total RMS power dissipation (P)	16.8mW

Table 5.5 Simulated DC performance.

5.6.2 Start-Up

Figure 5.26 shows the results of a transient simulation of the oscillator start-up. In this simulation, an impulse occurs on the power supply from 0V to 1.8V at 1ns and the oscillator amplitude reaches full scale within 9ns after this impulse. Figure 5.28 shows the first clock output, indicating that the frequency divider circuits are designed correctly. The clock signal swings rail-to-rail. Some initial meta-stable behavior is observed while the oscillator core is starting up. This behavior would be problematic when starting-up a processor. However, this problem can be addressed with the introduction of a synchronizer.

(a)   (b)
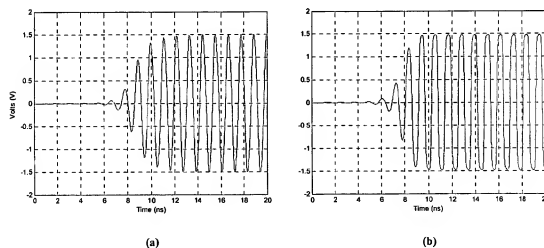
Figure 5.26 Oscillator start-up simulation. (a) Voltage across tank before. (b) RF amplifier output.

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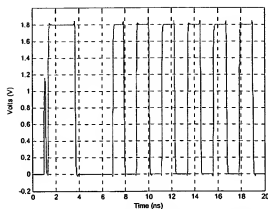
Figure 5.28   Simulation of frequency divider output waveform of the first divided clock.

5.6.3 Short Term Stability

5.6.3.1 Phase Noise

Phase noise was simulated using *Cadence*'s *SpectreRF* simulation tool. Results are shown in Figure 5.27 and summarized in Table 5.6 where these results are compared with the theoretical prediction given by (5.88). The theoretical data presented in Table 5.6 based on (5.88) is for the case $f_m = 100\text{kHz}$, $C_{eq} = 4.64\text{pF}$, $I_{tail} = 5.4\text{mA}$, and $R_P = 270\Omega$. Both (5.85) and (5.87) are required for evaluation of (5.88). Parameters for (5.87) include $L = 6.03\text{nH}$, $k = 8.62 \times 10^{-23}\text{J/K}$, and $T = 300\text{K}$. In (5.85), $\gamma = 3$, $\mu_p = 0.0058\text{cm}^2/\text{V-s}$, $\mu_n = 0.026\text{cm}^2/\text{V-}$
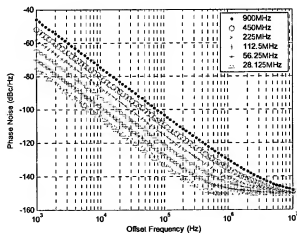
Figure 5.27   Simulated phase noise PSD for all clock frequencies.

Frequency (MHz)	Sim./theor. phase noise at 100kHz (dBc/Hz)	Sim./theor. calculated jitter (fs)	Sim./theor. calculated jitter (ppm)	Sim./theor. phase noise at 10kHz (dBc/Hz)	Sim./theor. calculated jitter (fs)	Sim./theor. calculated jitter (ppm)
896.90	-103.3/-106.7	—	—	-74.7/-76.7	—	—
448.45	-109.2/-112.7			-80.7/-82.7		
224.23	-115.3/-118.7			-86.8/-88.7		
112.11	-121.3/-124.7			-92.8/-94.7		
56.06	-127.2/-130.7			-98.7/-100.7		
28.03	-133.1/-136.7			-104.6/-106.7		

Table 5.6 Simulated phase noise summary. Jitter is estimated from phase noise using (2.67).

s, $W_p = 150\mu m$, $L_p = 0.25\mu m$, $W_n = 100\mu m$, $L_n = 0.25\mu m$, $V_{GSn} = |V_{GSp}| = 0.7V$ and $V_{Tn} = |V_{Tp}| = 450mV$. If (5.88) were evaluated at 10kHz, the phase noise would simply be 20dB greater than it is at 100kHz. However, at a 10kHz offset frequency, flicker noise upconversion from the tail device is observed. The frequency at which the flicker noise knee occurs can be determined from (2.43), or it can be estimated by setting the thermal noise power equal to the flicker noise power for the tail device and solving for the frequency. Flicker noise and thermal noise is modeled in *SPICE* by the following two expressions respectively,

$$\frac{\overline{i_f^2}}{\Delta f} = \frac{K_f I_D^{af}}{C_{ox} L_{eff}^2 f} \text{ and } \frac{\overline{i_d^2}}{\Delta f} = \frac{8}{3} kTg_m \qquad (5.106)$$

where $\overline{i_f^2}/\Delta f$ is the flicker noise current power, $\overline{i_d^2}/\Delta f$ is the channel thermal noise power, K_f is the flicker noise coefficient, af is the flicker noise exponent, and all other terms are as defined previously. The knee can be estimated by setting the two expressions equal and solving for f giving,

$$f = \sqrt{\frac{3K_f I_D^{af}}{8kTg_m C_{ox} L_{eff}^2}} \qquad (5.107)$$

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Using (5.107) and the relevant process parameters, it can be shown that the flicker noise knee falls near 100kHz. Using (2.43) yields a similar result. Thus, the theoretical flicker noise at 10kHz can be estimated by adding 30dB to the result found by evaluation of (5.88) at 100kHz. These results are also presented in Table 5.6.

The theoretical expression in (5.88) gives results quite close to simulation for 100kHz offset frequencies and the modification to account for flicker noise upconversion at 10kHz also yields quite accurate results.

5.6.3.2 Jitter

As shown in [43], jitter can be challenging to simulate where very long simulation times are required with a small transient step size. Thus, in this work, the jitter is estimated from phase noise at both 10kHz and 100kHz offset frequencies using (2.67). Results from theory and simulation are close. It should be noted that the jitter predicted from (2.67) will be an underestimate. This is because the assumption associated with the use of (5.88) is that the entire phase noise PSD can be modelled by a Lorentzian function. In fact, this is merely an estimate of the largest portion of the phase noise PSD. As was shown in Figure 2.8, the phase noise PSD has several regions with differing behaviors. Also worth noting is that the jitter estimated from (2.67) involves the conversion of a measurement on a logarithmic scale (phase noise) to a metric on a linear scale (period jitter). Consider that a 3dB error in phase noise results in a factor of two difference in the calculated variance. Therefore, accuracy within an order of magnitude is certainly reasonable.

5.6.4 Long-Term Stability

Long-term stability cannot be simulated accurately and thus these results are left to measurement.

5.6.5 Rise/Fall Times and Symmetry

The rise and fall times were determined using transient simulation results. A program was developed that takes the resulting time-domain data and detects the waveform points that are at 90% and 10% of the supply rail. Then the rise and fall times are computed between
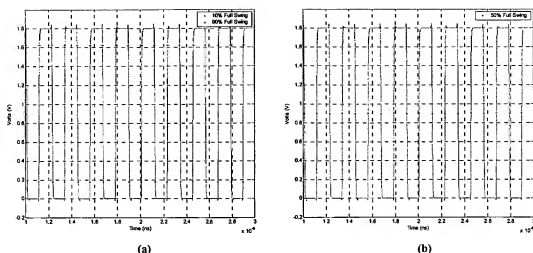
Figure 5.29 A program was developed to process transient simulation data. The program detects rise/fall times and duty cycle. (a) Time-domain waveform illustrating tagged 10% and 90% of full-scale voltages. (b) Time-domain waveform illustrating tagged 50% of full-scale voltage waveforms.

these detected points using the polarity of the slope of the line between the points which indicates whether the edge is rising or falling. Similarly, the duty cycle was determined by detecting the voltage waveform positions at which the signal was 50% of the supply rail and then computing the high and low pulse widths and taking the ratio of these figures. Figure 5.29 illustrates the transient data that has been tagged in order to determine the rise/fall times and duty cycle of the 450MHz clock output which is the first clock signal output. Using this technique, the results presented in Table 5.7 were determined.

Frequency	High/low waveform symmetry	Rise/fall time (ps)
448.45MHz	50.5/49.5	63.2/75.4
224.23MHz	50.2/49.8	63.2/75.4
112.11MHz	50.1/50.9	63.2/75.4
56.06MHz	50/50	63.2/75.4
28.03MHz	50/50	63.2/75.4

Table 5.7 Summary of clock voltage waveform symmetry and rise/fall times.

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5.6.6 Tuning Range

The clock synthesizer tuning response to bias current was simulated by varying V_{ctrl} to the current mirror and measuring the output frequency. Results are shown in Figure 5.30 versus the mirror supply current, along with the theoretical tuning response predicted by (5.53). The frequencies shown have been normalized to the measurement data that will be presented in subsequent sections. The simulated tuning range is 1.5%. The linear nature of the response predicted by (5.53) originates from the fact that the I_D in (5.53) was estimated by a scalar multiple of the current in the biasing mirror (N in Figure 5.23). However, this estimation does not model variation in the V_{DS} of the tail current device that feeds the amplifier. The V_{DS} variation causes the relationship between the current mirror bias and the tail current to be nonlinear. Thus, the simulation is more accurate because this bias variation is modeled.

A theoretical prediction of the tuning range can be determined using (5.47). $A_{max} = 4$ because this overdesign corresponds to the baseline overdesign with $V_{ctrl} = 0$. As before, $R_P = 270\Omega$, $C_{eq} = 4.64\text{pF}$, and $\omega_o = 2\pi\times900\text{Mrad}$. Using these variables, the predicted tuning range is 2.3%.
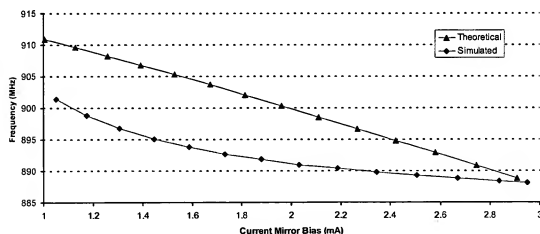
Figure 5.30   Simulated and theoretical oscillator core tuning response with varying current. The simulated tuning range is 1.5%.

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5.6.7 Frequency Accuracy

At this point, frequency accuracy can be determined only between analytical and simulation results. Simulation results predict an oscillation frequency of 896.9MHz. Analytical results predict 902.4MHz. Assuming that the theoretical frequency is the reference, the frequency accuracy is 0.61%. Higher frequency accuracy between simulation results and measured results is expected.

5.6.8 Power Supply Sensitivity

Frequency variation with the power rail was simulated for 1.8V±300mV. Results are shown in Figure 5.31 were the simulated sensitivity were 8.1%. Also shown in Figure 5.31, is the theoretical frequency variation with bias as determined by (5.67) and (5.104). Again, these results have been normalized to the measured frequencies that will be presented later.

These results can be compared to the derived theoretical expression for bias sensitivity given by the product of (5.66) and (5.98).

$$S_{V_{DD}}^{\omega_r} = -\frac{2V_{DD}}{(V_{DD} - V_T)} \frac{L}{8\left(\frac{R_P}{1-A}\right)^2 C_{eq}} \left(1 - \frac{1}{1-A}\right) \tag{5.108}$$
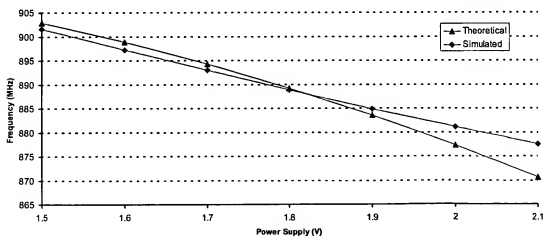
Figure 5.31   Simulated and theoretical power supply sensitivity for V_{DD}=1.8±300mV. The simulated power supply sensitivity is 8.1%.

The variables required for evaluation of (5.108) include: $V_{DD} = 1.8$V, $V_T = 450$mV, $L = 6.03$nH, $C_{eq} = 4.64$pF, $A = 4$, and $R_P = 270\Omega$. Using these design variables, the theoretical sensitivity is 7.1%, which is quite close to the simulated results. It is also worth noting that the polarity of the theoretical power supply sensitivity and the simulated sensitivity are the same.

5.6.9 Temperature Sensitivity

Temperature sensitivity was measured for two cases. In the first case, the clock synthesizer was biased at the typical operating point and measurements were made on the core frequency over temperature while the bias was allowed to free-run. In the second case, the current mirror bias was varied such that the current remained constant within the oscillator core. This latter test permits data to be collected independent of temperature variations in the bias circuitry. All simulations were conducted over the range of 0°C to 100°C.

Results from these simulations are presented in Figure 5.32, along with the theoretical prediction given by (5.76) and (5.105), where results are again normalized to the measured frequencies, which will be presented later. Here it can be seen that the simulated temperature sensitivity is positive for both cases. In the free-running case, the sensitivity is 0.26%, or 87ppm/°C, while in the constant current case it is 0.24%, or 80ppm/°C. These results can be compared to the theoretical predictions given by (5.73) which requires use of (5.66) and (5.103). In (5.66), $L = 6$nH, $R_P = 270\Omega$, $C_{eq} = 4.64$pF, and $A = 4$. In (5.103), $R = 50\Omega$, $\beta' = 2.2\times10^{-3}$, $I_D = 3$mA, $V_{DD} = 1.8$V, $V_T = 450$mV, $T = 300$K, $TC_1 = 2.9\times10^{-3}$. In (5.73), $TC_1 = 3\times10^{-4}$ and $T = 300$K. Using these numbers, the temperature sensitivity for the free-running bias is -0.31%, or -127ppm/°C. For the constant current bias condition, the sensitivity is -0.38%, or -150ppm/°C. Clearly there is a serious discrepancy between the simulation results and the theoretical prediction. In fact, the polarity of the sensitivities is opposite. It was determined that this was due to the fact that inductor temperature dependence has not been modeled in the *TSMC* 0.18μm design kit. It will be shown that the theoretical predictions are much closer to the measured data and the simulation results are incorrect.
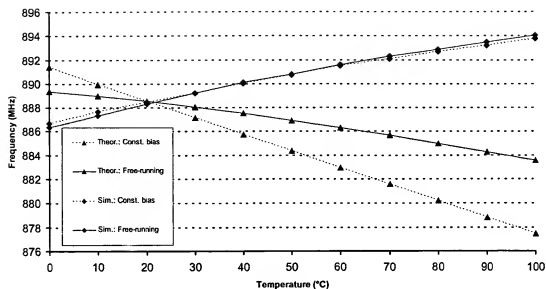
Figure 5.32 Simulated and theoretical temperature sensitivity of the oscillator core with a constant and free-running bias.

5.7 Measured Performance

A die micrograph of the fabricated clock synthesis circuit is shown in Figure 5.33a. The total die area is less than $1mm^2$, including bonding pads. Without bondings pads, the area is less than $0.3mm^2$. Initial functionality was tested by probing the several die, as pictured in Figure 5.33b, using a *Cascade Microtech* RF-1 microwave wafer probe station and ACP GSG-100 probes. Final tests were conducted on packaged parts, shown in Figure 5.33c, where a 16-pin dual inline package (DIP) was utilized. These packages did cause some loading the signals to be measured, as will be shown. The packages parts were mounted on a custom PCB as shown in Figure 5.33d. The PCB also contributed to the loading effects observed. Measured results are reported in the sections that follow and are compared to both theoretical predictions and simulation results. It will be shown that good agreement is found between both theory and simulation as well as theory and measurement.

5.7.1 DC Conditions

Table 5.5, on the following page, summarizes the measured DC measurements for the system.

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| (a) | (b) |
| (c) | (d) |
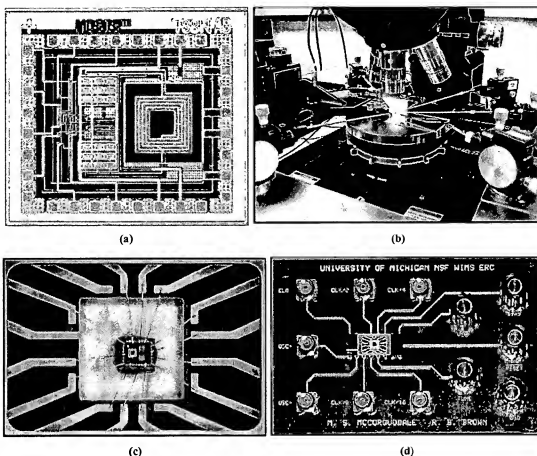
Figure 5.33   (a) Die micrograph of the fabricated clock synthesizer. (b) Probing the die with a *Cascade Microtech* RF-1 wafer probe station. (c) Die mounted and bonded into a 16-pin dual in-line package (DIP). (d) PCB with packaged die soldered into board for test.

Variable	Value
Power rail (V_{DD})	1.80V
Reference current (I_{ref})	2.91mA
Total RMS current not including I/O (I_{total})	8.80mA
Total RMS power dissipation (P)	15.8mW

Table 5.8 Measured DC performance.

5.7.2 Short-Term Stability

5.7.2.1 Phase Noise

Phase noise measurements were made with an *Agilent* E4405B Spectrum Analyzer with the 1D5 high-stability frequency reference option and the vB1.31 Phase Noise Personality.
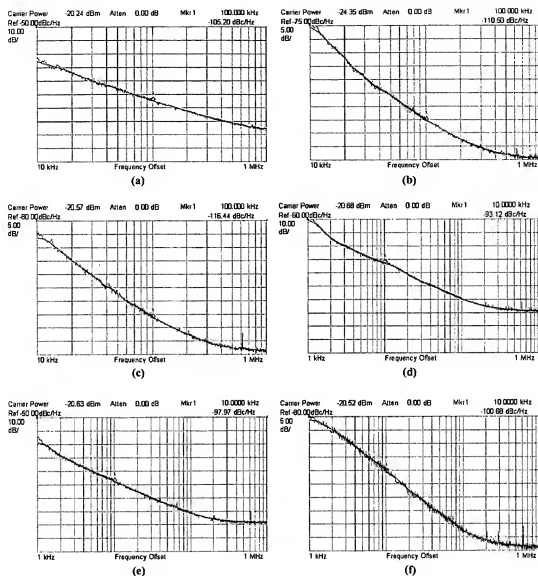
Figure 5.34   Phase noise power spectral density of the fundamental frequency for all clock outputs. (a) 891MHz. (b) 446MHz. (c) 223MHz. (d) 112MHz. (e) 56MHz. (f) 28MHz.

Measurements were averaged over ten samples. Signal tracking was not enabled, in order to measure any potential wandering of the synthesized clock.

The measured phase noise PSD for the fundamental frequency of all outputs is presented in Figure 5.34. As the clock signal is divided to lower frequencies, it becomes difficult to measure the phase noise at large offset frequencies because the phase noise has nearly rolled off completely. Similarly, for very high output frequencies, it is difficult to

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Clock frequency	Phase noise at 100kHz offset (dBc/Hz)	Phase noise at 10kHz offset (dBc/Hz)	Meas./theor. improvement (dB)
891MHz	-105.2	—	—
446MHz	-110.5	—	5.3/6
223MHz	-116.4	-87.0	5.9/6
112MHz	—	-93.1	6.1/6
56MHz	—	-98.0	4.9/6
28MHz	—	-100.7	2.7/6

Table 5.9 Summary of phase noise improvement due to frequency division.

measure the close-to-carrier phase noise PSD. Thus, the marker in Figure 5.34 is set at 100kHz offset for high-frequency clock signals and at 10kHz for low-frequency clock signals. Measurements are reported at both offsets for the intermediate frequency, 223MHz.

It is also worth noting that the phase noise at offset frequencies larger than 100kHz was difficult to measure even for high oscillation frequencies because of the limited power delivered by the output driver. As can be seen in Figure 5.34, for almost all output frequencies, the phase noise PSD flattens out at offset frequencies below 1MHz. Thus, measurements near 1MHz are not accurate. Consequently, all measurements are made at 100kHz or closer.

Recall that for each frequency division by a factor 2, the phase noise PSD is expected to decrease by 6dB. This improvement can be clearly seen in the measured data and is summarized in Table 5.9. Only for the case of the last frequency division was this 6dB improvement not observed. This was likely due to a layout problem that caused this output to be particularly sensitive to the logic switching nearby.

The power at which the oscillator core operates on the edge of the voltage-limited regime is approximately 5mW. This point can be determined by varying the current mirror bias point, V_{ctrl}, and monitoring the point at which the oscillation output power decreases on the spectrum analyzer. For the 891MHz output frequency, the measured phase noise power at 100kHz offset was -105.2dBc/Hz. The corresponding figure of merit (FOM), as defined by (4.28), is thus -177. This performance can be compared to the FOM of the previous work reported in Table 4.7. The only fully integrated work in CMOS where the

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reported performance is better than this work is [57] where the *FOM* is -178, a difference that is nearly negligible. All other previous work is in either bipolar, BiCMOS, or uses external components such as MEMS devices or bond wire inductors.

5.7.2.2 Jitter

In the most general sense, jitter can be measured in the time-domain with the infinite persistence mode of a digital sampling oscilloscope (DSO). Most DSOs support a statistics mode with a histogram function that can be configured to measure the variation in the edge positions of the signal over time. Unfortunately, the measurement is not this trivial. In fact several factors must be considered when measuring the period jitter. First, in order to display the signal on a DSO, the signal must be self-triggered. The internal clock of the instrument cannot be used to trigger the signal because the signal to be measured and the internal clock are both autonomous and thus not synchronized. Consequently, the signals will drift past each other in time due to both short-term and long-term instabilities. However, self-triggering presents a problem because the trigger position will also jitter. This problem can be resolved by assuming that the trigger jitter and the jitter of the next subsequent edge are uncorrelated, which is an appropriate assumption for an autonomous oscillator as described in Chapter II. With this assumption, the variance (measured jitter squared) of the two measurements can be subtracted, or specifically,

$$J = \sqrt{J_1^2 - J_T^2} \tag{5.109}$$

where J is the period jitter of the device under test (DUT), J_1 is the jitter of the first period after the trigger, and J_T is the jitter of the trigger event.

Additional complications in the measurement include the fact that the internal time base of the DSO also jitters and thus this jitter also adds to the total jitter measured. Of course this jitter is uncorrelated with the jitter of the DUT and thus its associated variance can also be subtracted from there measured jitter. There exists a technique by which this jitter can be determined. Referring to (2.49), the accumulating jitter increases by $\sqrt{n}$ for each nth transition beyond the trigger point. The accumulated jitter can be measured and the slope of the line can be compared to this theoretical prediction. The difference between the

measured slope and the theoretical slope is the jitter of the time base. This approach was utilized in this work and it was found that the time base jitter is very small as compared to the jitter of the DUT. Thus, correction due to time base jitter is not introduced here.

Aside from these concerns, an additional complication associated with the instrumentation arises when measuring jitter. In this work, as with much previous work, jitter is measured with a *Tektronix* DSO. These DSOs contain an internal time delay between the trigger event and the displayed waveform. Thus the event that caused the trigger cannot be observed unless the measurement signal is delayed as shown in Figure 5.35. This delay can be achieved with a power splitter and an appropriate length of cable, but it can be difficult and time consuming to estimate the delay associated with the added cable length. Moreover, it is often difficult to find the correct edge on the oscilloscope. In theory, this edge will be the edge with the least amount of variance. However, being a statistical measure, jitter cannot be calculated accurately unless sufficient samples have been collected over an appropriate period of time. Collection of the data takes a substantial amount of time and thus it can be very time consuming to identify the appropriate edge. Unfortunately for frequency synthesis systems that exhibit both accumulating and synchronous jitter, such as a PLL, this measurement approach is the only option available. However, for the developed synthesis system, the jitter is predominately accumulating. Thus, the difference of the variance between any two subsequent measures after the trigger event can be used to determine the actual jitter. To prove this, begin by considering a DUT with jitter J and a trigger jitter J_T. The variance of the nth edge away from the trigger is given by,
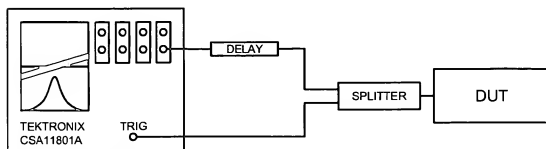
Figure 5.35   Typical jitter measurement set-up using a DSO in infinite persistence mode. The scope is triggered by the DUT. A delay line is introduced in order to overcome the internal delay of the DSO and observe the trigger event.

$$J_n^2 = nJ^2 + J_T^2 \qquad (5.110)$$

The jitter measured on the subsequent edge is given by,

$$J_{n+1}^2 = (n+1)J^2 + J_T^2 \qquad (5.111)$$

and thus the difference of the variance between the two edges is given by,

$$J_{n+1}^2 - J_n^2 = J^2 \qquad (5.112)$$

where clearly this difference gives the actual variance of the DUT and thus a delay line is not required in order to observe the trigger. In fact, the jitter of the DUT can be determined from the difference of the variance between any two arbitrary and subsequent edges after the trigger event. This makes the measurement substantially easier as compared to the delay-line approach described previously.

A *Tektronix* CSA11801A with an SD-22 low-noise high-speed sampling head was used to measure the clock jitter. The period jitter is then calculated using the following expression, which was just verified.

$$J = \sqrt{J_{n+1}^2 - J_n^2} \qquad (5.113)$$

Measurements were made on subsequent edges and at least 50,000 samples of data were collected for each edge. Typically, more than 15 minutes was required for each measurement. An example of the data collected for subsequent edges of the slowest clock is shown in Figure 5.36 where the number of "Hits" indicates the number of samples in the histogram. For both measurements, this is greater than 50,000. The measurement indicated by RMSΔ is the RMS jitter of the edge and simply the standard deviation of the histogram data. In Figure 5.36a, the jitter is 5.912ps. In Figure 5.36b, the jitter is 6.231ps. The root of the square difference gives 1.97ps. All measured results are summarized in Table 5.10, along with the phase noise results presented previously and the predicted jitter.

The total amount of jitter increases with frequency division as predicted and the ppm jitter decreases. The theoretical reduction factor for each frequency division by 2 is

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$1/\sqrt{2}$, or 0.71. As can been seen in Table 5.10, the measured reduction factor is very close to the theoretical prediction. Also in Table 5.10, jitter is estimated from the measured phase noise data using (2.67). Clearly (2.67) provides only a rough estimation of the actual jitter. As expected, the measured jitter is higher than predicted due to flicker noise and other noise not modelled in (2.67). Nevertheless, the conversion is a useful estimation and the general trend is similar to measurement in the sense that ppm jitter is reduced by frequency division. A more accurate estimation of jitter from phase noise could be obtained using (2.78), but unfortunately the *Agilent* E4405B does not support data point output from the phase noise personality and thus a numeric integration technique could not be employed. Certainly a graphical technique could be explored, but such an endeavor does not serve much purpose. Jitter can be roughly estimated from phase noise using (2.67), and it can be measured accurately using the time-domain approach described here. The behavior observed is the same for both approaches.

(a)   (b)
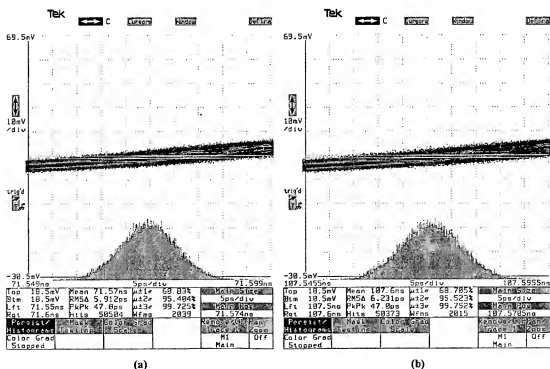
Figure 5.36   Histogram data for subsequent edges of the 28MHz clock. The actual jitter is computed by taking the root of the difference between the square of the RMS variation. Measured jitter is thus 1.97ps. (a) First edge jitter=5.912ps. (b) Second edge jitter=6.231ps.

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Clock Frequency	Measured jitter (ps/ppm)	Meas./theor. Jitter reduction (ppm)	Phase noise PSD at 10kHz (dBc/Hz)	Predicted jitter from phase noise (ps/ppm)
446MHz	0.64/280	—	-77.0	0.15/67
223MHz	0.74/170	0.61/0.71	-87.0	0.13/29
111MHz	1.2/130	0.76/0.71	-93.1	0.19/21
56MHz	1.7/94	0.72/0.71	-98.0	0.30/17
28MHz	2.0/56	0.60/0.71	-100.7	0.62/17

Table 5.10   Summary of measured jitter improvement due to frequency division. Also shown is predicted jitter from measured phase noise PSD using (2.67).

5.7.3 Long-Term Stability

The long-term stability was determined by testing the free-running oscillator for 24 hours and measuring the frequency variation. Over this period the frequency varied by 1kHz from the start-up frequency. Extrapolating this data linearly over time results in 0.25% variation in the clock frequency in approximately 6 years.

5.7.4 Rise/Fall Times and Symmetry

Do to the limited drive capability of the output stages, the rise and fall times are dominated by loading of the instrumentation and thus any measured data is not representative of the true rise and fall times on chip. For example, the 223MHz clock signal is shown in the time-domain in Figure 5.37. The measured rise and fall times are almost four times that predicted by simulation, which is clearly due to loading. In subsequent renditions of this clock synthesis system, larger output drivers can be used in order to determine these metrics.

Waveform symmetry, however, could be measured easily using the *Tektronix* DSO. Referring to Figure 5.37 again, it can be seen that the duty cycle is almost exactly 50%. In fact, the measured duty cycle was almost exactly 50% for all output clock signals.

5.7.5 Tuning Range

The oscillator was tuned using the frequency pulling approach presented previously. The bias current in the oscillator core was modulated by varying V_{crtl} in the current mirror.
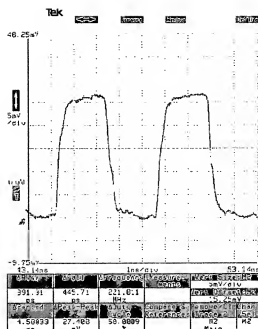
Figure 5.37 Sample time-domain 223MHz clock waveform captured using a *Tektronix* CSA11801A and the *Wavestar* GPIB instrument data capture software package.

Results from test are reported in Figure 5.38 along with the previously presented theoretical and simulation data.The measured sensitivity is 3.0%. The derived analytical expression in (5.66) predicts a sensitivity of 2.7%, which is in very good agreement with measurement.

The measured tuning range is 2.2%. As will be shown in the next section, the frequency accuracy is well within 2%, this tuning range is sufficient to achieve frequency
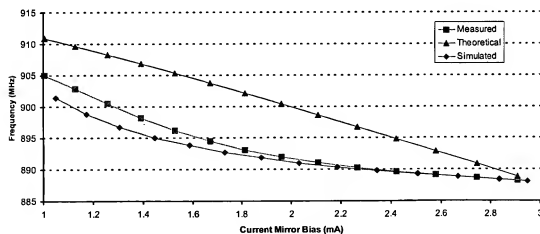
Figure 5.38 Measured, theoretical, and simulated frequency tuning. Measured sensitivity is 3.0% and the measured tuning range is 2.1%.

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accuracy within 0.25% or less, corresponding to the frequency accuracy required for applications such as USB 1.1 [112]. Using the theoretical expression in (5.47), the predicted tuning range is 2.3%. Simulation results predicted a tuning range of 1.5%. Both results are close to the measured data.

5.7.6 Frequency Accuracy

The oscillator core frequency was measured across 20 die at ambient temperature. Results are shown in Figure 5.39. The mean measured frequency is 891.4MHz with a maximum deviation of 0.75%. As shown in Figure 5.39, two outlying points are what dominate the frequency accuracy. If these two points are not included, the mean frequency is 890.73MHz with a peak deviation of 0.33%. This out-of-fab frequency accuracy is very high for a monolithic clock and coupled with the tuning mechanism described in the previous section, opportunities exist in applications where very high frequency accuracy is required.

Simulation results predicted an oscillation frequency of 896.9MHz, corresponding to 0.62% accuracy as compared to the measured mean frequency. Similarly, analytical expressions predicted an oscillation frequency of 902.4MHz, corresponding to 1.2% accuracy as compared to the measured mean. Both simulation and analytical results are quite close to measured results and tuning permits enough control to correct the variation.
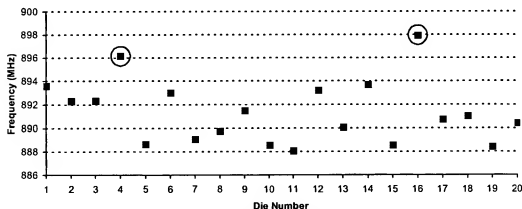
Figure 5.39   Measured frequency of the oscillator core across 20 die. Two outlying points are circled. Including these points, accuracy is within 0.75%, Not including these points, accuracy is within 0.33%.
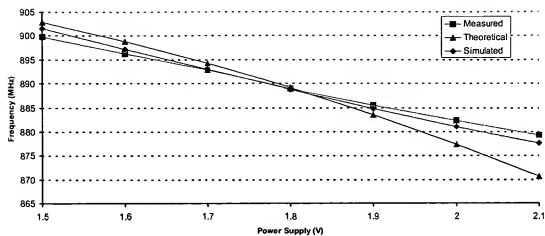
Figure 5.40 Measured, theoretical, and simulated power supply sensitivity for V_{DD}=1.8V±300mV. The measured power supply sensitivity is 6.9%.

5.7.7 Power Supply Sensitivity

The sensitivity of the oscillator core frequency to variations in the power supply rail was tested by varying the V_{DD}. Results are shown in Figure 5.40 along with the theoretical and simulation results presented previously. The measured sensitivity is 6.3%. Using the derived analytical expression, which is the product of (5.66) and (5.98), the sensitivity is predicted to be 7.1%. Simulation predicts 8.1%. Both analytical and simulation results are quite close to measured results.

Certainly this sensitivity is quite high and it is mostly due to the high sensitivity of the current mirror. This current mirror could be replaced by a band-gap or similar reference and then the sensitivity could be reduced greatly. However, in this work, a simple current reference was utilized in order to test and verify frequency tuning by varying the oscillator current. In future renditions, a mechanism will be required that can stabilize the current with V_{DD} but also provide current tuning.

5.7.8 Temperature Coefficient

Again, temperature sensitivity was measured for two cases. In the first case, the clock synthesizer was biased at the typical operating point and measurements were made on the core frequency over temperature while the bias was allowed to free-run. In the second case, the

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current mirror bias was varied such that the current remained constant within the oscillator core. All measurements were made in a temperature and humidity controlled oven over the range of 0°C to 100°C.

Figure 5.41 shows the results from measurement along with the theoretical and simulation results presented previously. For the case where the bias is free-running, the temperature sensitivity is -0.19%, corresponding to a temperature coefficient in ppm of −77 ppm/°C. For the case where the current is fixed to a constant current, the temperature sensitivity is -0.22%, corresponding to a temperature coefficient in ppm of -88ppm/°C. Using the derived analytical expression in (5.75) temperature coefficients of -127ppm/°C with the current mirror free-running, and -150ppm/°C with constant current, are predicted. Simulation results predict 87ppm/°C with the current mirror free-running and 80ppm/°C with the current fixed. It was determined that simulation results are erroneous due to the fact that the available design kit did not model inductor temperature dependence. The analytical predictions are close to measured results. Discrepancies arise due to changes in the amplifier transconductance through mobility and the threshold voltage. In both cases, the temperature sensitivity was overestimated by (5.75). Including the sensitivity of these two variables in the analysis would increase the accuracy of the analytical predictions, although
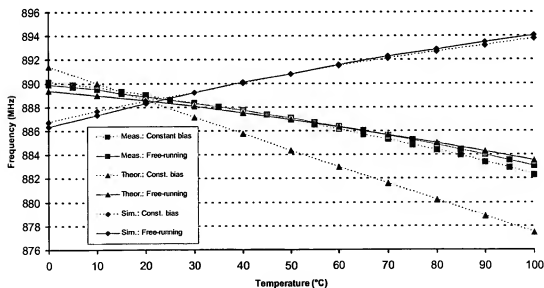
Figure 5.41   Measured, theoretical, and simulated temperature sensitivity of the oscillator core with free-running and constant bias.

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such an analysis is quite lengthy. Nevertheless, the derived expressions demonstrate the two most significant factors that affect the frequency sensitivity to temperature which are the variation in the inductance and the bias variation.

A temperature compensation technique is straightforward. In fact, when the current mirror bias is left free-running, it begins to compensate the variation due to the inductor. This is because the bias current in the mirror decreases over temperature as the bias resistor increases over temperature. As has been shown, bias current and frequency have a negative sensitivity. Thus, as the bias current decreases, the frequency increases, which compensates for the variation in the inductance. Of course, the compensation provided by this configuration is insufficient, but it is obvious how a compensation technique can be implemented. Simply, the current in the core needs to be reduced as temperature increases. This can be achieved with a kT/q current reference where an appropriate fraction of the kT/q current is subtracted from the core as temperature increases.

5.7.9 Microphonic Sensitivity

Microphonic sensitivity was not measured because the current implementation is all silicon with no mechanical parts. Thus, the synthesizer should be nearly immune to microphonics.

5.7.10 System Metrics

System metrics are summarized in Table 5.11 in the following section.

5.8 Summary and Conclusions

A summary of all theoretical, simulated, and measured metrics is presented in Table 5.11. Very good agreement was observed between both theoretical predictions and measured data, and simulation results and measured data, with one exception. The temperature sensitivity simulation was grossly in error due to an apparent model parameter extraction error for the inductor.

This prototype has demonstrated the viability and performance of a top-down harmonic monolithic clock synthesis system. Performance results are outstanding. Some

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Metric	Theoretical prediction	Simulation result	Measured/actual data
Short-term frequency stability: Phase noise at 10kHz (dBc/Hz) a. 891MHz b. 446MHz c. 223MHz d. 112MHz e. 56MHz f. 28MHz	a. -76.7 b. -82.7 c. -88.7 d. -94.7 e. -100.7 f. -106.7	a. -74.7 b. -80.7 c. -86.8 d. -92.8 e. -98.7 f. -104.6	a. — b. -77.0 c. -87.0 d. -93.1 e. -98.0 f. -100.7
Short-term frequency stability: Phase noise at 100kHz (dBc/Hz) a. 891MHz b. 446MHz c. 223MHz d. 112MHz e. 56MHz f. 28MHz	a. -106.7 b. -112.7 c. -118.7 d. -124.7 e. -130.7 f. -136.7	a. -103.3 b. -109.2 c. -115.3 d. -121.3 e. -127.2 f. -133.1	a. -105.2 b. -110.5 c. -116.4 d. — e. — f. —
Short-term frequency stability: Jitter (ps/ppm) a. 446MHz b. 223MHz c. 112MHz d. 56MHz e. 28MHz	Est. from phase noise at 10kHz a. b. c. d. e.	Est. from phase noise at 10kHz a. b. c. d. e.	a. 0.64/280 b. 0.74/170 c. 1.2/130 d. 1.7/94 e. 2.0/56
Short-term frequency stability: Jitter (ps/ppm) a. 446MHz b. 223MHz c. 112MHz d. 56MHz e. 28MHz	Est. from phase noise at 100kHz a. b. c. d. e.	Est. from phase noise at 100kHz a. b. c. d. e.	a. 0.64/280 b. 0.74/170 c. 1.2/130 d. 1.7/94 e. 2.0/56
Long-term frequency stability (ppm/day)	—	—	1.1
Rise/Fall times (ps)	—	63.2/75.4	—
Waveform symmetry (worst case)	—	50.5/49.5	51/49
Tuning range	2.3%	1.5%	2.2%
Bias current sensitivity	2.7%	3.0%	2.8%
Frequency accuracy a. Core frequency, f_o (MHz) b. Absolute error (rel. meas.) c. Variation	a. 902.4 b. 1.2% c. —	a. 896.9 b. 0.62% c. —	a. 891.4 b. — c. $f_o \pm 0.75\%$
Power supply sensitivity	7.1%	8.1%	6.9%

Table 5.11 Summary of theoretical, simulation, and measured performance metrics.

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Metric	Theoretical prediction	Simulation result	Measured/actual data
Temperature coefficient (ppm/°C) a. Free-running b. Constant current	a. -127 b. -150	a. 87 b. 80	a. -77 b. -88
Microphonic sensitivity	—	—	—
System metrics a. Size b. Process technology c. Power dissipation, no I/O, (mW)	a. — b. MM/RF CMOS c. 16.2	a. — b. MM/RF CMOS c. 16.8	a. 1mm^2 b. MM/RF CMOS c. 15.8

Table 5.11 Summary of theoretical, simulation, and measured performance metrics.

results that stand out in particular are the out-of-fab frequency accuracy, the temperature stability without compensation, and the jitter. The performance reported here is far superior to any ring, phase-shift, or relaxation approach reported.

Despite the advances reported here, there remain several areas for further study and improvement. First, the power dissipation is relatively high. Compared to a crystal and PLL approach, the power dissipation is likely less. However, compared to a ring oscillator approach, the power dissipation is likely ten times higher, if not more. The developed prototype was overdesigned and thus in future renditions, the power can be scaled back substantially. Additionally, architectural considerations can be explored. For example, this *LC* clock oscillator could be enabled when a processor is running at full speed. However, when the processor enters a sleep mode, this clock could be disabled and a ring oscillator could be activated, thus saving power.

Other areas for future research include power supply stabilization techniques and temperature compensation. Techniques for both have already been proposed here in this work and are relatively trivial. The trivial nature of these techniques stems largely from the stable performance of the clock synthesizer even without compensation. The task that remains at hand is the development of this clock synthesis block into a processor or microcontroller application. This is the topic of the next chapter.

CHAPTER VI

DESIGN AND IMPLEMENTATION OF

MONOLITHIC CLOCK SYNTHESIS IN AN

EMBEDDED MICROSYSTEM

I N CHAPTER I, both environmental and biological testbeds were described as applications for this research. These testbeds require support for signal acquisition and signal processing. A modified version of the clock synthesis technology developed in Chapter V has been incorporated into a microsystem that has been developed for these sensor applications. The design of this system is presented here.

Both microprocessors and microcontrollers have become ubiquitous in electronic applications. However, the systems supported by these devices have become exceedingly complex in terms of functionality and the number of peripheral components that must be supported. For example, the end-to-end system architecture for the testbeds includes sensors and actuators, signal conditioning, data conversion circuitry, a microprocessor, memory, a wireless interface, and supporting electronics including the system clock reference. In previous research, the boundaries of these systems have stretched to include several peripheral components on a common substrate, marking the advent of system-on-chip (SoC) and microsystem development.

Microsystem boundaries have been expanded even further in this work, while a focus has been maintained on key design constraints including power, size, and performance. These metrics have been considered particularly within the context of the environmental and biological testbeds. The developed microsystem includes an analog front end

(AFE) that supports data conversion and signal conditioning while operating at 900mV. With the use of the clock synthesizer described in Chapter V, the clock synthesis function has been merged on-chip to reduce overall system complexity by eliminating the off-chip crystal reference and on-chip PLL. Lastly, a highly efficient low power instruction set has been combined with architectural power reducing techniques to ensure minimal power dissipation in the digital core.

In the sections that follow, the design methodology, simulation performance, and test data for this microsystem are presented. The development of this system has been a collaborative effort and has lead to advances in the area of microsystem design methodologies and techniques. These approaches, reported here, are an extension of current mixed-signal research. However, the work presented in this dissertation is the first instance in which micromachined, analog, and digital electronics have been combined within a complete and exhaustive design framework.

6.1 Architecture and Anatomy of the Microsystem[1]

The microsystem was developed with a focus on sensor control applications, but retains enough flexibility for a variety of other general-purpose uses. Shown schematically in Figure 6.1, the microsystem is comprised of three major subsystems: a digital core, an analog front end, and a monolithic clock synthesizer. The core consists of an efficient 16-bit, three-stage pipeline with 64KB on-chip static random access memory (SRAM). A timer and multiple serial interfaces were included in order to communicate with external devices. The AFE conditions an analog input signal, typically from sensors, and performs analog-to-digital conversion before sending the conversion results to the core. The clock synthesizer supplies the digital core and AFE with a low-jitter, frequency selectable, and tunable clock signal while requiring less power than an off-chip crystal reference and on-chip PLL. The entire microsystem would ideally operate at 900mV, however currently only

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1. The ISA for the microcontroller described in this section was developed by Matthew R. Guthaus. The hardware implementation of this microcontroller was developed by Robert M. Senger and Eric D. Marsman and the USART was developed by Dan J. Burke. The analog front end was developed by Fadi H. Gebara and Keith L. Kraver.
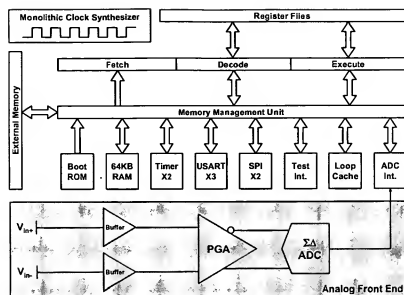
Figure 6.1 Microsystem functional architecture including a 16-bit processor core, analog front end, and monolithic clock synthesizer.

the AFE has been designed for this extremely low supply voltage. The digital core supply is limited to 1.8V because the SRAM and digital libraries are characterized at this voltage. Potential future research certainly includes migration of the digital core and the clock synthesizer to a 900mV supply.

6.1.1 Microcontroller

6.1.1.1 Core

A 16-bit load/store architecture with dual operand register-register instructions was chosen to satisfy the power and performance requirements of the microsystem. The 16-bit datapath was selected to reduce the complexity and power consumption of the core while providing adequate precision in calculations given that the sensors controlled by this chip typically require 12 bits of resolution. The datapath pipeline consists of three stages: fetch, decode, and execute. Typically in sensor applications, processing throughput requirements are minimal. Moreover, in most sensing systems, power dissipation is a key design constraint and clock frequencies should be kept as low as possible. A three-pipeline-stage architecture was chosen to obtain acceptable performance at low clock frequencies while also maintaining design simplicity.

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A 24-bit address space for unified data and instruction memory was used to satisfy the potentially large storage requirements of remote sensor systems. The 16MB of supported memory is byte addressable and provides sufficient storage for program, data, and memory-mapped peripheral components in a single address space. The current implementation of the core has 64KB of on-chip SRAM with an off-chip memory bus interface to allow full utilization of the remaining memory space. Multiple peripheral components and a 256-byte boot ROM share the memory space.

The machine contains sixteen general-purpose data registers and four address registers, all of which are split into two windows each containing eight data and two address registers. The windowing scheme permits instructions to be encoded in 16 bits by reducing the number of bits required to encode register operands. Three additional non-windowed address registers (a stack pointer, frame pointer, and link register) are used by the compiler for subroutine and stack support. The hardware supports one level of interrupts via two registers that store the Program Counter (PC) and Machine Status Register (MSR). Interrupts are maskable and prioritized up to 64 different levels.

6.1.1.2 Instruction Set Architecture

The instruction set architecture (ISA) includes 77 instructions and 8 addressing modes. The addition of bit-manipulation instructions allows for bits in memory to be set/reset in two cycles via one instruction instead of separate read, mask, store instructions that would otherwise be required. Two-word instructions were necessary to support 24-bit absolute addressing modes with 16-bit instructions. Address update modes provide for easy manipulation of the addresses stored in the address registers by allowing both pre- and post-update operations. Load and store instructions are available with or without update and in word or byte mode. Standard arithmetic and logical instructions are included along with support for multi-word add and subtract operations. The multiply and divide instructions take multiple cycles to complete and are available with single or two word results and source operands. For hardware simplicity, they are implemented by shifting and accumulating results using the ALU instead of with dedicated functional units. Subroutine and conditional change-of-flow instructions are included along with special test instructions.

6.1.1.3 Memory Architecture

By subdividing the memory structure into different blocks, at the cost of extra area for duplicated sense amps and other peripheral circuitry, a memory structure was obtained that dissipates less power than a monolithic memory. Using the *Artisan* SRAM compiler for the 0.18μm process available from *Taiwan Semiconductor Manufacturing Company*, the optimal configuration for 64KB of on-chip memory was determined to be eight banks of 8KB each. This topology allows one to disable all single-port memory banks that are not being accessed on a cycle-by-cycle basis. It also allows a single instruction and data access to different banks of memory on the same cycle without stalling the pipeline. A dedicated memory-management-unit in the core routes data from the correct bank to the requesting unit and disables inactive banks of memory. The memory speed is sufficient to allow all accesses to complete within one cycle without the need for caches. As a power saving feature, a modified loop cache as shown in [113] was added to the chip. The loop cache is not a true cache, but rather is a small, low power, 512-byte memory that is pre-loaded with the most commonly executed instructions (typically loop code) or frequently accessed data as determined through compiler profiling. This greatly reduces the power consumption of the controller since embedded controllers typically run the same software throughout their lifetime and much of that time is spent executing loop code.

6.1.1.4 Peripherals

Supported peripherals include two universal synchronous asynchronous receive/transmit (USART) units, a 12-bit general-purpose parallel output port, a Serial Peripheral Interface (SPI) unit and a multifunction programmable timer. One USART is dedicated to communication with external components, the other is for general use and for loading programs into memory. The SPI is ideal for communicating with multiple sensors that share a single sensor bus, as presented in [114]. The timer is capable of timing both internal and external events. With these peripheral components easily accessible through software, communication with the microsystem is both versatile and efficient.

6.1.1.5 Functional Verification

An extensive environment was developed using Perl scripts to facilitate functional verification of the digital core. Focused assembly language test cases were used to test the basic operation of each instruction in the ISA, as well as anticipated corner cases. Additional test cases were written with the sole purpose of verifying interrupts and the timing of peripherals such as the USART, SPI, and timers. A random assembly code generator was developed and used to generate millions of lines of random test cases. Random tests detected functional bugs that might have been missed in the focused test cases, particularly any unexpected interdependencies between instructions as they progressed down the pipeline. The same verification process was repeated after logic synthesis in *Synopsys Design Compiler* and again after automatic place and route (APR) in *Cadence Silicon Ensemble*, exposing functional bugs that might have been introduced by the synthesis/APR tools.

6.1.1.6 Performance Estimation

The digital core consists of 120,000 transistors, excluding SRAMs. Using *Nanosim* it was estimated that the core will dissipate 7mW at 66MHz. The switching vectors used by *Nanosim* were obtained by running assembly language test cases on the *Verilog-XL* simulator and capturing the resulting switching activity. The power associated with a read or write to one of the 8KB SRAM banks is significant (specific numbers are proprietary to *Artisan*), while the leakage and standby power are very small for this process. RAM power dominates the digital logic power. However, due to design time constraints, use of a standard RAM generator was the only option. Future research certainly includes power-intelligent RAMs in order to achieve reduced power dissipation. Another improvement would be to use non-volatile FlashROM for instruction memory.

6.1.2 Analog Front End

6.1.2.1 Overview

The analog front end (AFE) consists of three major components: buffers, a programmable gain amplifier (PGA), and a 2nd-order $\Sigma\Delta$ modulator. Each component has unique features

that are highlighted in this section. General design considerations are discussed first to motivate the design decisions.

6.1.2.2 Design Considerations

The AFE has been designed to operate at supply voltages ranging from 900mV to 1.8V. In this work, the feasibility of a 900mV system using current technologies is demonstrated. For the targeted sensor applications, a 100Hz Nyquist conversion speed with a resolution of 12 bits is sufficient. The interface to the sensors should be high impedance with near-zero current draw. With these requirements, many issues in architecture and circuit design arise that would not ordinarily be encountered.

The AFE was developed using a differential architecture. This offers the advantages of increased substrate noise rejection, reduced effects of charge injection and most significantly, increased signal swing. To understand the importance of signal swing, consider a single transistor abstraction of an amplifier in a switched-capacitor circuit. It can be shown that power, P, is proportional to dynamic range, DR, and inversely proportional to the supply voltage, V_{DD}, [115]. Consider the following expression,

$$P \propto kT \cdot DR \left(\frac{V_{gs} - V_t}{\alpha^2 V_{DD}} \right) f_s \qquad (6.1)$$

where $\alpha^2 V_{DD}$ $(0 < \alpha < 1)$ is the signal swing, f_s is the sampling frequency, k is Boltzmann's constant, T is temperature, and $V_{gs} - V_t$ is the device overdrive voltage. This clearly shows the importance of maximizing signal swing in a reduced supply voltage environment. Therefore, most circuits comprising the AFE must support rail-to-rail input and output stages.

A switched capacitor (SC) approach was employed in the AFE, as it offers superior matching, inherent linearity, and implementation efficiency. The switch used in an SC circuit consists of both n-type and p-type MOSFETs as shown in Figure 6.2a. If V_{DD} is greater than the sum of the threshold voltages then the switch operates properly as illustrated in Figure 6.2b. However, if V_{DD} is less than the sum of the threshold voltages, a region exists

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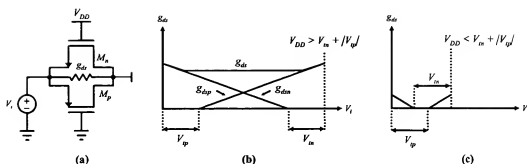
Figure 6.2 Switch conductance as a function of supply voltage. (a) A general CMOS transmission gate. (b) Switch characteristic for high supply voltage. (c) Switch characteristic for low supply voltage.

in which the switch does not conduct as shown in Figure 6.2c. When operating at 900mV this poor conduction situation arises, thus requiring unique circuit design techniques.

6.1.2.3 Buffers and Programmable Gain Amplifier

In a data acquisition system, such as an AFE, a signal conditioning stage is usually required. Typically, programmable gain amplifiers (PGAs) are used to adjust the signal amplitude level before an analog-to-digital conversion. This adjustment ideally maximizes the input signal range of the analog-to-digital converter. The PGA, shown in Figure 6.3, consists of two main components; a fully differential switched operational amplifier and a variable SC
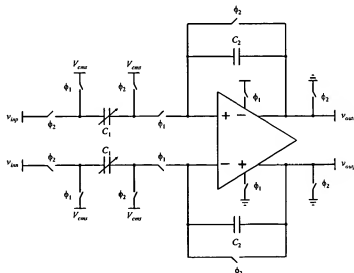
Figure 6.3 Architecture of the switched capacitor (SC) programmable gain amplifier (PGA).

Design Parameter	Simulated Value
Unity gain bandwidth (MHz)	3.6
Open loop gain (dB)	96
Phase margin (degrees)	55
High/low output swing (V/V)	$0.020/V_{DD}$
PSRR at DC (dB)	102
CMRR (dB)	128
Power (μW)	40

Table 6.1 Simulated performance for the programmable gain amplifier.

feedback network. In [116], the switched-opamp technique has been shown to enable low-voltage SC circuits. In this work, the switched-opamp technique is applied to the PGA, which permits removal of the input sampling switches of the ADC, thereby enhancing the dynamic range. The gain is programmed by switching capacitors in parallel with the input sampling capacitor of the feedback network. During the sampling phase, ϕ_1 is ON and ϕ_2 is OFF, the opamp is enabled and the output voltage is proportional to C_1/C_2. During the second phase, ϕ_1 is OFF and ϕ_2 is ON, the opamp is disabled and the output of the PGA is pulled to ground. The reference voltage, V_{cms}, must be low enough to enable sufficient overdrive and conductance of associated switches. Typically, the variable sampling capacitor, C_1, is implemented as multiple capacitors selectively connected in parallel with a switch. These switches should be placed on the top plate of the sampling capacitors so that the input signal swing is not limited. Also, most switches in this circuit are not required to pass a mid-rail voltage, thus making this architecture ideal for low-voltage applications.

The fully differential operational amplifier that was used in the development of the PGA includes a class AB input stage and a class AB rail-to-rail output stage. The performance characteristics are summarized in Table 6.1. Resistive common-mode feedback was used because it does not limit the output swing. Also, it should be noted that devices biased in weak inversion were used to permit operation at low-voltage levels.

The switches at the input of the PGA were implemented using a switched operational-amplifier technique which provided two benefits. First, the switched operational-

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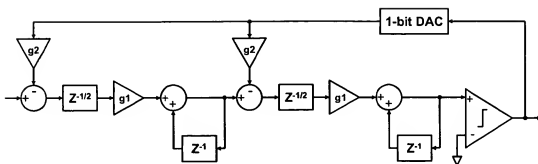
Figure 6.4   Architecture of the 2nd order ΣΔ modulator.

amplifier is capable of passing mid-rail signals and second, it provides a high impedance buffer between the PGA and the input.

6.1.2.4 2nd-Order ΣΔ Modulator

A second order ΣΔ modulator, illustrated in Figure 6.4, was chosen because of a superior trade-off between resolution and bandwidth as compared to oversampling alone. The ΣΔ topology utilizes feedback to provide noise shaping, thus pushing the quantization noise produced by the 1-bit ADC to higher out-of-band frequencies. Because the sensor application calls for a low Nyquist rate and a resolution of 12 bits at low power, this ADC was the optimal choice. The feedback also reduces the requirements on the performance of the analog circuits, making this architecture suitable for implementation in deep-submicron digital processes. Since the ΣΔ modulator represents the digital data in a pulse-code-modulated (PCM) format, digital filtering is needed. The filtering, which is done through software on the microcontroller, removes the out-of-band noise and recovers the digital data. A summary of the performance characteristics of the ADC is shown in Table 6.2.

6.1.3 Monolithic and Top-Down Clock Synthesizer

6.1.3.1 Overview

The clock synthesizer has been thoroughly described in Chapter V and the design implemented in this microsystem is nearly identical. The version implemented in this microsystem operates at a slightly higher frequency. Additionally, a much broader range of clock frequencies are synthesized, from 1.1 GHz to 2 kHz. The details are described next.

Design Parameter	Simulated Value
Effective number of bits	11.5
Voltage full scale (mV)	850
SNDR with a full scale input (dB)	71
Power (μW)	10

Table 6.2 Simulated performance for the 2nd-order $\Sigma\Delta$ modulator.

6.1.3.2 Design Considerations

Considering the target applications discussed previously, it is clearly desirable to operate the microcontroller in a low power standby mode when only minimal processing is required. Of course dynamic power dissipation in the microcontroller is directly proportional to the switching frequency of the logic, which is dependent on the clock frequency. Thus, very low clock frequencies are required. As mentioned above, it is desirable to switch the clock frequency in a single cycle, which is very difficult to achieve with a PLL, but can be done with the clocking technology developed in this work. However, a serious concern is presented by the potential for clock glitches that might occur when the clock frequency is changed abruptly. These glitches could cause the processor to enter an unpredictable state. This concept in illustrated by the timing waveform in Figure 6.5. Here the output clock is switched from a clock signal at one frequency to a clock signal at twice the original frequency. As shown, a very narrow glitch can occur depending on the timing of the signal on select line and this glitch may well be too fast for the subsequent logic to process. An even more serious problem would arise if the next logic stage becomes meta-stable due to the glitch.

A simple approach was implemented in order to address the problem just described. Specifically, all clock signals were derived from a reference clock that operates at twice the fastest frequency of the processor. This reference clock originates from the clock synthesizer module. The highest frequency at which the processor was developed to operate is 66MHz and thus a 132MHz signal from the synthesizer is required. From this single signal, 16 frequencies are generated, the highest of which is 66MHz and the lowest of which is approximately 2kHz. The typical operation frequency of the microsystem is 33MHz. All
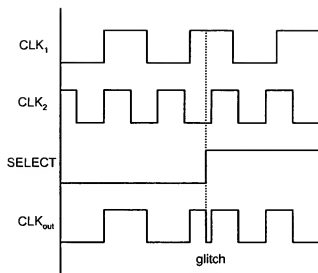
Figure 6.5   Timing waveform illustrating the possibility of a glitch when switching instantaneously between two clocks of different frequencies.

are related in frequency by integer multiples of two and thus each one can be generated using a simple flip-flop divider as was shown in Chapter V. The single reference signal from the synthesizer also clocks a series of five synchronizers as shown in Figure 6.6. Thus, the actual clock that feeds the processor logic is selected by a clock that operates at twice
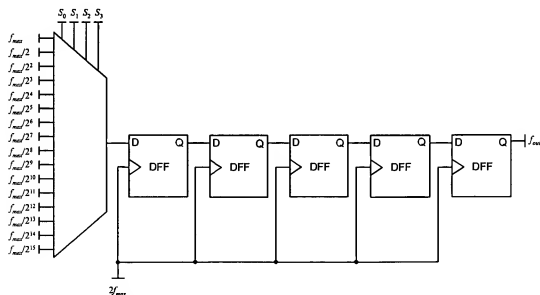
Figure 6.6   System schematic for clock frequency selection. The 5 synchronizers prevent glitches from occurring on the output clock line. Additionally, all selected clock signals are timed by a clock that operates at twice the fastest frequency that can be selected for the processor.

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Design Parameter	Simulated Value
Power supply rail (V)	1.8
Bias current (mA)	9.0
Power dissipation (mW)	16.2
Output frequency (MHz)	33.0
High/low voltage output level on-chip (V/V)	1.8/0
High/low voltage output level off-chip (V/V)	3.3/0
10%-90% Voltage rise/fall time (ps)	52/61
Duty cycle (high/low)	50/50
Phase noise PSD at 10kHz offset (dBc/Hz)	-92
Period jitter (ps)	1.9

Table 6.3 Simulated performance parameters for the monolithic and top-down clock synthesizer.

the frequency of any of the clocks that can be selected. This approach also mitigates any potential problem that can arise from glitches. It can be shown that the mean time to failure for the clock output designated by f_{out} in Figure 6.6, is extremely long [117].

In order to achieve the frequencies desired, the reference frequency was set to approximately 1.1GHz, which is higher than the operation frequency of the design presented in Chapter V. The frequency increase required a corresponding increase in bias current in order to ensure start-up of the reference oscillator. Also, the frequency increase requires modification of the LC tank. The inductor was not modified, but rather the net capacitance in the tank was reduced by eliminating 6 capacitors from the array and thus the total tank capacitance was 5.5pF as opposed to 8.3pF.

6.1.3.3 Performance Estimation

Performance metrics were simulated for the 33MHz clock signal because this is the nominal operation frequency for the microsystem. Results are presented in Table 6.3. The performance of the clock at other frequencies can be estimated using the frequency translation relationships presented in Chapter III.

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Simulation results were acquired using the approaches presented previously in Chapter V. The simulated phase noise density of the 33MHz clock was -92dBc/Hz at 10kHz offset. Period jitter was calculated from (2.67) and scaled by $\sqrt{2}$ because this offset frequency is above the oscillator line width. The estimated jitter was 1.9ps. Time domain and DC performance was determined with the simulation environment and data processing techniques described in Chapter V. A summary of these performance parameters is given in Table 6.3.

The clock reference supply voltage is 1.8V in order to interface to the digital core. However, the supply voltage could be scaled to 900mV. This is because oscillator start-up is based on current and not voltage.

6.1.4 Design for Test

Many testability features have been incorporated into the digital core to facilitate post-fabrication functional testing. Most notable is the Test Interface, which is a modified USART that provides read or write access to any one of the internal system registers through specialized test instructions. The test interface supports the injection of an instruction into the pipeline and then single-stepping that instruction through the pipeline. Additionally, the test interface provides the benefit of testability using little more than a notebook computer with a standard RS-232 serial port. This will be particularly valuable for verifying sensor systems in the field.

At-speed testing of the fabricated digital core was performed using an HP82000 digital IC tester. The same test cases that were used in simulation have been converted into test vectors and will be run through the HP82000 tester. Initial tests will be loaded into the tester memory and fetched through the chip's external memory bus. A special feature was integrated into the boot ROM so that when an external interrupt is asserted during boot-up, the external interrupt handler in the boot ROM immediately jumps to an address in external memory (in this case it will be mapped to the tester memory). This bypasses the remainder of the boot ROM and most importantly, allows testing of the chip even if the on-chip memory is not functioning. An additional testability feature includes hardware breakpoint modes to assist in stopping the microcontroller accurately.

Testing of the AFE was performed through external probe points. Visibility and overdrive pads were added at the outputs of the buffers, PGA, and the $\Sigma\Delta$ modulator. This allows for an input signal to be traced through the AFE into the microcontroller at crucial points. Also, all current and voltage reference points were made externally visible for monitoring. The output of the ADC, in PCM format, is accessible externally for recording and subsequent signal processing in *Matlab*. The internal clock synthesizer signal has been routed to the padframe for tester accessibility. Additionally, an external clock input has been included for diagnostics. The microcontroller contains a programmable multiplexor that selects between the monolithic synthesizer and the external clock. The monolithic clock frequency and time domain stability will be measured using external instrumentation.

6.1.5 Summary

The previous sections have outlined the basic microsystem design and performance parameters. In the sections that follow, a detailed design methodology for the microsystem is described. First, an IP-based design approach is presented where the microsystem is considered as the sum of several IP blocks. Following that discussion, a complete top-down design and bottom-up verification approach is described.

6.2 An IP-Based Design Approach

6.2.1 Motivation

It has recently been estimated that semiconductor design productivity is increasing at a rate of 28% annually while semiconductor capacity is increasing at a rate of 58% annually [118]. This trend quantifies the now well-known productivity-capacity gap in semiconductor development. Many electronic design automation (EDA) tools have been developed to reduce this gap, but one particular solution that has received significant attention is design reuse through intellectual property (IP) [119]. For example, it has been reported that application specific integrated circuit (ASIC) design productivity increased by a factor of 2.5 from 1996 to 2000 while system-on-chip (SoC) development productivity increased 7 times within the same timeframe. Most of the gains realized in SoC development have been

attributed to IP design and reuse, clearly indicating the importance of IP to accelerating design time and increasing design productivity [120].

Although the benefits associated with IP design and reuse are clear, the challenges of its use are many. Reports in the field point to the importance of IP repositories and a standardized IP framework for IP component development [121]. Indeed a lack of these repositories and standards, both internal and external to organizations, is a significant bottleneck toward IP use and design productivity acceleration [122]. Industry has clearly identified this problem and is taking strides toward its solution where several commercial IP repositories now exist such as the *Virtual Component Exchange* (*VCX*) and *Design & Reuse*. However, research institutions have not yet pursued similar initiatives.

In the development of this microsystem, each functional unit has been converted into an IP block and then instantiated into the microsystem, using techniques that will be described in subsequent sections. Additionally, 3rd party IP has been incorporated into the microsystem, including the SRAM and bonding pads. This microsystem marks one of the first IP-based research designs of this scope where full-custom IP blocks including analog, digital, and mircomachined components are merged with large-scale commercial IP blocks.

6.2.2 IP Formats and Nomenclature

IP can be categorized into three application formats: functional, infrastructure, and platform [123]. The corresponding IP can then be delivered as either hard, firm, soft, or design methodology IP. In the sections that follow, a review of the basic definitions of these formats is presented. Illustrations of these IP formats are presented in Figure 6.7 and Figure 6.8.

6.2.3 Application Formats

6.2.3.1 Functional IP

IP components that provide, support, or implement specific operations are functional IP. Microprocessors, memory, analog amplifiers, and MEMS are all examples of functional IP. This application format currently comprises the bulk of commercially available IP.
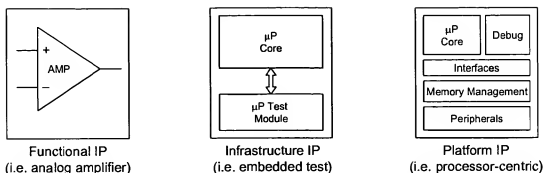
Figure 6.7   Application formats for intellectual property: functional, infrastructure, and platform. Several different IP types exist for each application format.

6.2.3.2 Infrastructure IP

Infrastructure IP supports development, characterization, configuration, debugging, and test of electronic systems. Some examples of infrastructure IP include embedded test modules, mask level interconnect for gate array definition, and design methodologies.

6.2.3.3 Platform IP

Platform IP is an emerging application format in which the IP is developed and delivered as a larger functional component that can be customized through the addition of newly developed peripherals or other IP components. Commercial entities such as *ARM Ltd.* deliver several microprocessor product lines as a platform where the CPU, operating system, and peripheral components are pre-defined. In essence, platform-based design is a development foundation, or baseline, for designing an SoC or microsystem for a particular application [124]. Platform-based design can be of several topologies, where the *ARM* platform described previously is processor-centric. Other approaches include communications-centric, program-centric, and application-centric.

6.2.4 Delivery Formats

6.2.4.1 Hard IP

Hard IP is the physical design of a particular IP component and thus is process specific. It is delivered as GDS or some other physical design format. Hard IP is the least customize-

able, but the most reliable IP format because verification of hard IP includes specific timing and electrical information that is specific to the manufacturing process. For this reason, hard IP is also the best option for closing the productivity-capacity gap as it can be used without additional internal component verification, although intermodule verification is still required.

6.2.4.2 Firm IP

Firm IP is a netlist or register transfer language (RTL) description of an IP component. Physical design for digital circuits can be compiled from firm IP with a place and route tool. As an optional prior step, the firm IP may be synthesized for any process technology without modification to the functionality of the original component. The advantage of firm IP to the user is that it is not process specific.

6.2.4.3 Soft IP

Soft IP is the most easily customized IP format as it is described by a hardware description language (HDL), such as *Verilog*. Soft IP can be synthesized to firm IP with a tool such as *Synopsys Design Compiler*. The firm IP can then be compiled to hard IP. However, considering that verification is at least 50% of the design cycle for IP components, soft IP might be an excellent option for customization, but it is not a good option for closing the productivity-capacity gap [125]. When many custom modifications are pursued, the component must be verified again.
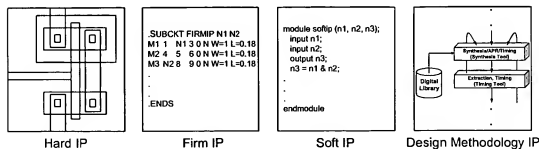
Figure 6.8   Delivery formats for intellectual property: hard, firm, soft, and design methodology.

6.2.4.4 Design Methodology IP

Design methodology IP is a format that has been identified as critical to microsystem and SoC development. It is a type of infrastructure IP that is utilized within the design framework. Examples include design flow and framework documentation and scripts that modify data files for use across tool suites.

6.2.5 IP-Based Platform Design Assembly

The microsystem was developed using a processor-centric platform-based design approach. The processor core and associated peripherals were developed and synthesized together from soft IP. Synthesis was achieved with the standard cell library for the *TSMC* 0.18μm process available from *Artisan Components Inc*. These components comprise the IP-platform, or baseline processor. The 64KB on-chip memory banks and loop cache were generated from *Artisan*'s memory compilers. The AFE and clock reference components were then instantiated and routed as hard IP components, as shown in Figure 6.9.
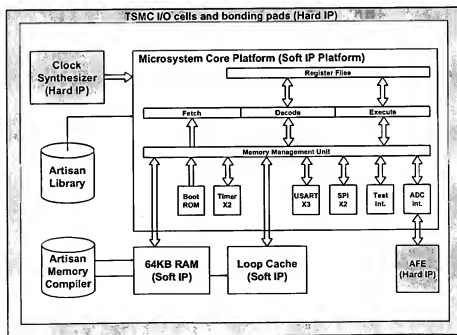
Figure 6.9   Processor-centric platform IP structure. The AFE and clock synthesizer designs, along with the I/O cells, are hard IP while all other IP is soft.

Each IP component was created and verified individually, and then system was assembled at the top level. A *Verilog* description of the top-level connections, top-level buffering, an abstract of the IP in the standard LEF, and the standard process and routing layer information were used by *Silicon Ensemble* to automatically place and route the top-level design. *RC* extraction was performed for final simulation verification purposes.

The ghost views of the hard IP components, standard cells, and memory components were replaced with GDS using the *Cadence Design Framework II. Mentor Graphics Calibre* was then used for DRC, ERC, and LVS.

6.2.5.1 Challenges

While IP reuse has several advantages over an original design effort, it is not without difficulties. Developing a design methodology that allows the EDA tools to understand the required attributes of each IP component is the first challenge. An intimate understanding of all of the data files and environment variables for the tools used is required in order to achieve the desired design performance and verification. However, once these required modifications are developed and documented, the data files required to describe any type of IP component, examples of these components, and a design flow that uses them with a complete suite of tools are easily accessible and understandable.

6.3 A Top-Down Design Methodology for Microsystems

Designing and verifying a complete microsystem involves several challenges as these designs include not only a union of the analog and digital circuit domains, but also the magnetic, mechanical, biological, chemical, or electrical domains. Moreover, the design constraints associated with systems such as these can be as specific as the material properties of a layer that defines a microstructure to as broad as an abstraction of the embedded processor that supports the firmware for the microsystem. A variety of tools for completion of such designs exist, but as yet, there is no complete end-to-end framework for development. In this work, advances in integrated circuit CAD tools are leveraged and coupled with trends in microelectromechanical systems (MEMS) and mixed-signal circuit design in order to address the challenges associated with the development of microsystems. Here an

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efficient and effective design methodology for such development is proposed. Additionally, the gaps that call for new design automation developments are identified.

6.3.1 Trends and Challenges Associated with Microsystems Technology

Fig. 6.10 illustrates a generalized end-to-end wireless integrated microsystem. Here the various technologies along with the typical design tools for each are illustrated. Tremendous breadth exists when developing such systems. For example, MEMS components are often developed with finite element (FE) tools that simulate mechanical response to an applied stimulus, while the microprocessor section is almost completely synthesized with some form of hardware description language (HDL). Digital IC design tools are now ubiquitous and offer the designer tremendous flexibility through system abstraction. Only recently have such trends developed in the analog and mechanical domains.

There are several existing and future MEMS technologies that warrant integration with CMOS or a related process technology. Indeed a great deal of research has been underway in this field including activities in monolithic MEMS-based oscillators [81], accelerometers [126], and switches [127], to name just a few. Only recently have such subsystems been developed, so ambiguity in a holistic design flow and gaps in the related CAD framework are not surprising. Clearly, a design methodology for such systems that addresses the
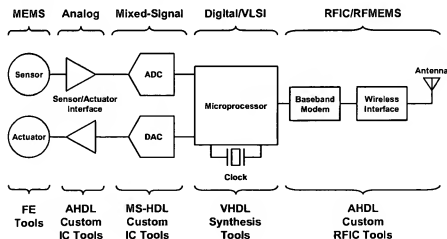
Figure 6.10   The anatomy of a generalized wireless integrated microsystem. Key technologies and associated development tools are shown.

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challenges associated with the convergence of these technologies is required if complete systems that implement these research breakthroughs are to come to fruition.

Current and past development approaches have been typically ad-hoc and bottom-up in nature. This design methodology is an outgrowth of both the disparate nature of the technology and the process by which this technology has developed. Much MEMS work to date has been focussed on device development. Once device performance is optimized, supporting electronics are added incrementally. Therefore, a bottom-up development approach is rather natural. However, now these devices are appearing within larger systems and the typical development strategy is to partition sections of the microsystem into the mechanical, analog, or digital domains. After partitioning, design activities become disjoint and ad-hoc, with each subsystem being designed using a separate tool suite, and with little, if any, cross-domain verification. As discussed previously, MEMS devices have been designed almost exclusively with finite element tools, however the majority of these simulators do not support an interface with a standard IC framework. Therefore, in almost all applications, some level of model extraction and abstraction is required for simulation of the MEMS component with the supporting analog electronics. Often, this extraction is customized to each component and it must be completed by the designer without the aid of design automation. Additionally, MEMS-based systems often require logic for programming or trimming, and in many applications a complete embedded processor is required to support the system. Standard tool suites allow designers to synthesize digital logic and physical design from a hardware description language, but typically verification is not performed with the analog and MEMS devices integrated into the microsystem. In fact, addressing the shortcomings associated with automated MEMS design has motivated the development of the software package that is described in Chapter VII.

As Figure 6.10 and the previous discussion illustrate, several disparate tools are required for the development of microsystems. Specific design challenges involve management of these tools as well as system verification across these various design platforms. Clearly, the number and complexity of tasks involved in the development of microsystems are significant. Attention to design methodology has become increasingly important in

order to develop systems efficiently and close the design gap between manufacturing and design capabilities [128].

6.3.2 Typical Bottom-Up Design Methodology

A bottom-up design methodology involves the development of each block from the device to system level. Devices are combined to form blocks, which are then combined to complete and verify the system. In [129], the problems associated with a bottom-up design methodology are addressed. They include lack of architectural study and optimization, costly redesign effort associated with iteration through the flow, and significant processing time for system-level simulation, if it is even possible.

Figure 6.11 illustrates this typical design methodology as applied to microsystems technology. Here a system specification is translated into a specification for three domains: digital, analog, and mechanical. Design activities ensue from the device to block level and from the block to system level. A macro is delivered from each domain and the system is assembled with an automatic place and route (APR) tool. The system is then verified and only at this point are problems addressed. Therefore, time-consuming redesign effort is
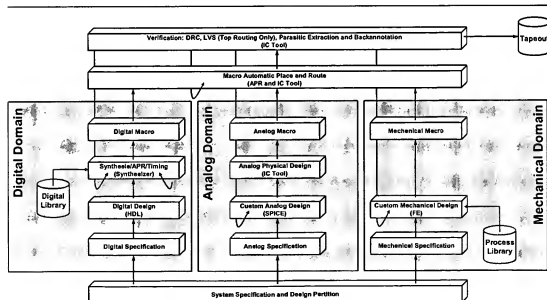
Figure 6.11   Typical ad-hoc and bottom-up microsystems design methodology. Design iteration is costly because verification does not occur early in the design flow, but rather at the system level. If iteration is required, it must occur back at the device level, thus substantially increasing design time.

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required back at the device level. Moreover, additional iterations are also common with the APR tool in order to optimize macro placement.

Although methodologies such as these have been employed in the past, they are clearly insufficient for complex microsystems. As the field matures, it is likely that microsystems will contain several, if not hundreds, of magnetic, mechanical, optical, chemical, or biological components along with the supporting analog and digital devices. A proper, efficient, and exhaustive design methodology and framework is obviously required.

6.3.3 Proposed Design Methodology: Top-Down

The proposed design methodology has been implemented in the development of a complete microsystem described previously.

6.3.3.1 A Top-Down Approach

In a top-down approach, development would proceed from the system to device level. The system could be studied and optimized with a mixed-signal HDL (MS-HDL) from which the abstract circuit blocks are derived. Device-level designs would then be completed, and achieved performance could be benchmarked against the original specification using the abstract blocks and system model. Throughout a top-down design methodology, cross-domain verification at various levels should be budgeted. This reduces the likelihood of time-consuming redesign effort at higher levels of system assembly.

In conjunction with the top-down approach, several additional development requirements were considered while constructing the design methodology. An environment that supports hardware abstraction and cross-domain simulation for MEMS, analog, and digital electronics was required. The environment also had to support simulation of abstract hardware with device primitives in order to accurately model digital programming of analog and mechanical components without synthesis of these digital devices. A model that could be modified easily for system verification based on the realized subsystem performance was desirable, as was cross-domain verification at every level of abstraction. The complete tool suite had to support low-level simulation including FE and basic transistor-

level analysis, as well as non-linear RF and noise analysis. Support for HDL synthesis, timing verification, and APR was mandatory for digital design and final chip assembly.

Although no single design framework met all of these design requirements, it was determined that the *Cadence AMS* environment is well-suited to achieving many of these goals for system-level development of microsystems technology. In particular, this environment supports *Verilog-AMS*, an analog and digital HDL which is a superset of the *Verilog* and *Verilog-A* languages. It was determined that *Verilog-AMS* is also ideal for behavioral modeling of mechanical devices. Prior to the emergence of *Verilog-A*, many MEMS engineers had been using device level models, including elementary circuit primitives, for MEMS component modeling. Clearly, the *Verilog-A* language is a significant improvement over this technique as it provides added modeling flexibility while it minimizes complexity.

Additional tools used in this work included *Spectre* for analog subsystem and transistor-level design, *Coventorware* for FE analysis of MEMS components, *Synopsys* for digital synthesis, *Cadence Silicon Ensemble* for APR, and *Mentor Graphics Calibre* for DRC and LVS. The requirement of such an extensive and disparate tool suite is a significant challenge faced in the development of microsystems technology.

6.3.3.2 Methodology

With a framework in place, a design methodology was determined, as illustrated in Figure 6.12. *Verilog-AMS* was employed to realize the system specification. MEMS and analog components were modeled in *Verilog-A*, while the microprocessor core and peripherals were modeled in *Verilog*. From this system model, a natural partition of top-down subsystem design activities followed. Each block was specified with an abstraction for the hardware. In parallel with behavioral verification of the digital section, the blocks in the mechanical and analog domains were developed and performance metrics were determined. Updated *Verilog-A* was developed to model achieved performance from FE simulation in the mechanical domain while device-level design and analysis using *Spectre* led to achieving the analog specification. The digital electronics were developed such that a complete behavioral description of the hardware was realized. At this point, the first cross-

domain verification of the system was achieved. Once the HDL from each domain had been updated with the achieved performance, verification of the system model was trivial. In the *Cadence AMS* environment, HDL and primitives may be mixed and critical subsystem performance metrics can be determined quickly with a detailed model for the subsystem and an abstract model for the remainder of the system. This was particularly significant when considering analog and MEMS device-level performance that required digital programming which was described only by HDL.

A system-wide simulation was completed and iteration in the mechanical and analog design activities continued, in order to achieve the target system performance. This first cross-domain simulation offered significant benefits over the bottom-up methodology described previously. First, design effort had not been expended synthesizing the digital
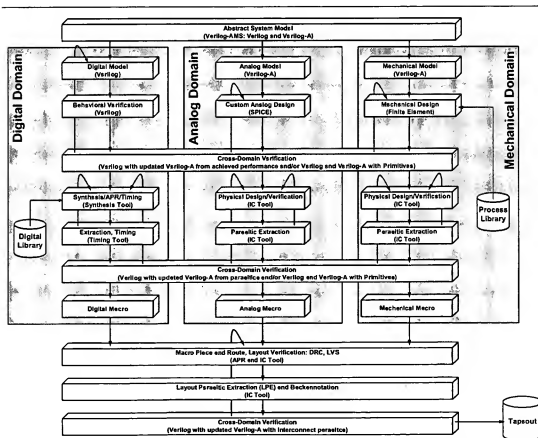
Figure 6.12 Proposed top-down microsystems design methodology. Design iteration occurs early in the methodology. Also, cross domain verification can be performed well before system integration.

electronics. Second, iteration in the design of the MEMS and analog circuits occurred early in the design flow. Last, the system simulation was fast as it was described by behavioral HDL, not a complete device-level netlist. However, simulation was also timely in the case of a primitive-level subsystem simulation as the remainder of the system is described by HDL and only the critical blocks were modeled at the device-level.

System development continued with a typical physical design methodology. The digital sections were synthesized and the mechanical and analog sections were custom designed. Timing information from the synthesis tool was used in an iteration to achieve timing closure for the digital section. Similarly, parasitic extraction and backannotation afforded an iterative process in completing the mechanical and analog sections. Once timing closure was reached in each domain, a second cross-domain simulation was executed for system verification based on physical design. Again, the HDL for the subsystems was updated and system simulation was timely and accurate. Physical design iteration continued until timing closure was achieved for the complete system. The domain-specific design activities completed with the delivery of a hard macro.

The final system development activities included APR, physical design verification (DRC, LVS), layout parasitic extraction (LPE), and backannotation. A final cross-domain verification was completed once parasitic extraction data for the interconnect between macros was determined. APR iteration was also necessary.

6.3.4 Gaps in the Tool Suite

Several CAD-related shortcomings were encountered throughout the development of this microsystem. All of these gaps are associated with the development of MEMS and analog electronics. First, the utilized design tool suite lacks support for a MEMS behavioral model that is automatically extracted from FE simulation. Likewise, an analog behavioral model that is automatically extracted from SPICE simulation is not supported.

Throughout the physical design flow, a lack of physical verification of the MEMS devices in primitive form was encountered. Synthesis libraries for MEMS and analog components from behavioral or topological models were also unavailable. As a result, porting microsystem designs between process technologies through synthesis is not achievable.

Several custom and elementary patches have been developed for these design gaps in order to automate design flow. For example, the lack of MEMS device verification was overcome by custom modification of the DRC and LVS decks. However, this activity can be quite complicated, particularly if the designer is unfamiliar with the deck syntax. Trivial fixes include *Verilog-A* models that were updated by hand from achieved performance in *Spectre*. However, this process becomes time-consuming when considering complex analog subsystems. Other similar patches were employed and automation of patches like these would greatly facilitate microsystem designs of the future.

Solutions to the other identified gaps are more difficult. Analog and MEMS synthesis from HDL or a topological model is indeed a significant endeavor. Nonetheless, some tools for this very purpose [130] are available today and active research in this field in underway such as work shown in [131]. With the use of such synthesis capabilities, the design would have been completed in a more timely manner. Consequently, a tool has been developed in this work to address the need for MEMS synthesis and it is presented in Chapter VII.

6.3.5 Physical Design

The physical implementation of the microsystem is shown in Figure 6.13. The die area is 12.8mm^2 and the transistor count is over 3.5 million. The microsystem includes two custom components of hard IP and one custom platform of soft IP. Third party IP includes the digital cell library, memory, loop cache, input/output drivers, and bonding pads. The developed microsystem includes digital, analog, mixed-signal, and micromachined components.

6.4 Test Results

A battery of tests was conducted on the microcontroller and each individual IP block was verified. The test results from the core, peripherals, and AFE are not presented here, but the results from the clock synthesis block are described next. These results are of significant interest because deployment of the developed clocking approach into a processor application is certainly the ultimate test of its utility. In fact, some concerns lie in the fact that nearby switching logic may affect the performance of the clock reference. Concerns such
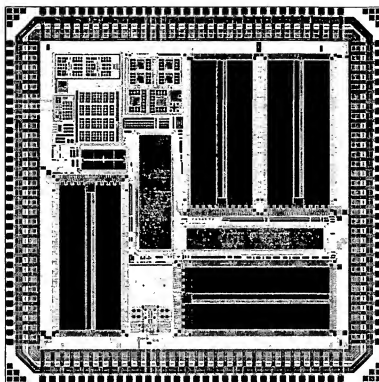
Figure 6.13 Physical design of the microsystem in *TSMC*'s 0.18μm MM/RF process. The design contains over 3.5 million transistors in an area of 12.8mm^2. The monolithic and top-down clock synthesis block is pictured at bottom, just left of center.

as these are addressed in the sections that follow. However, much of the measurement detail presented previously in Chapter V has been omitted here. The focus of this section is on the functional performance of the clock as the sole reference for the microsystem, glitch-free ultra-fast frequency switching, and the effects of noise on the clock signal due to the nearby logic switching.

6.4.1 Basic Functionality

The clock was first tested by verifying that the processor can be run from it and without any external clock. Using an HP82000 digital system tester, pictured in Figure 6.14, all of the instructions supported by the microsystem were tested using both the monolithic clock reference and the external clock reference from the HP82000. The processor executed all instructions correctly in both cases and thus the logic was determined to be fully functional. Moreover, it was verified that the microsystem can indeed be clocked from the monolithic

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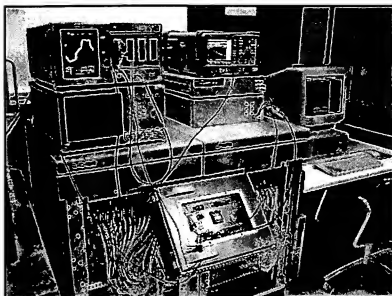
Figure 6.14   HP82000 test set-up. The packaged microsystem is positioned in the middle of the testing board. Time and frequency domain analyzers are positioned above the HP82000.

reference with the same logic performance that can be achieved with an off-chip crystal-based clock that is sourced from the HP82000. Millions of instructions were clocked at full speed using the monolithic clock reference and no error was observed.

6.4.2 Glitch-Free Ultra-Fast Frequency Switching

Of the many benefits associated with the developed architecture, the ability to achieve ultra-fast frequency switching is one of the most unique and interesting. In the following tests, the clock frequency is changed dynamically by loading the correct word into the multiplexer shown in Figure 6.6. Here, the measured time-domain data is presented.

Figure 6.15a shows the most typical application for frequency switching where the clock transitions from a low-frequency standby state to a high frequency processing mode. Figure 6.15a shows a glitch-free transition from 1MHz to 33MHz, corresponding to a nearly instantaneous frequency change by a factor of over 30. In fact, much broader changes can be achieved including the maximum transition from 2kHz to 66MHz, corresponding to frequency change by a factor of 33,000. However, it is difficult to capture these transitions with a sampling scope and in a manner that can be presented as in Figure 6.15a.
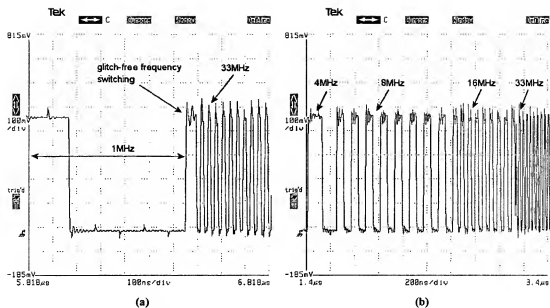
Figure 6.15 Time domain data captured with *Tektronix* CSA11801A sampling oscilloscope and the *Wavestar* GPIB acquisition software package. (a) Frequency switching from 1MHz to 33MHz. (b) Frequency switching from 4MHz to 8MHz to 16MHz to 33MHz.

It is worth noting that in Figure 6.15a, an intermediate period is observed, as is often the case. The clock selection line is asynchronous relative to the clock signals and thus the transition always occurs at a random point within the period of the lower frequency signal. Consequently an intermediate frequency is observed for one half cycle.

Measurements were also made for the case where the clock frequency was changed abruptly and rapidly. Figure 6.15b shows a measured waveform where the clock frequency transitions from 4MHz to 8MHz to 16MHz to 33MHz. Again, no glitches are observed. The transition between 16MHz and 33MHz appears to have some irregularity, but this arises from the display resolution of the oscilloscope.

6.4.3 Frequency Instability due to Logic Switching

The frequency stability of the 33MHz clock was tested under two conditions. In the first condition, the processor logic was stopped, but the clock tree remained on. The clock tree cannot be disabled because the clock must continue to run in order to process interrupt requests. Thus, a true off-state cannot be achieved. The second test condition was with the

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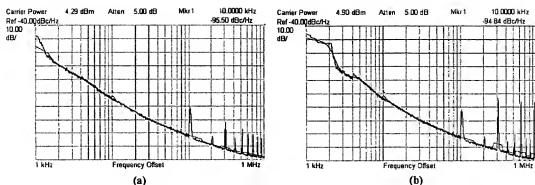
Figure 6.16   Phase noise measurement of the 33MHz clock signal acquired with the phase noise personality running on an *Agilent* E4405B spectrum analyzer. Data was acquired with the *Agilent IntuiLink* GPIB acquisition software package. (a) With the processor stopped. (b) With the processor running.

processor logic running a loop routine. Both phase noise and jitter measurements were acquired using the techniques presented in Chapter V. Phase noise results for the two conditions are shown in Figure 6.16. Here it can be seen that the logic switching increases the phase noise by less than 1dB. However, in both cases, spurious peaks are observed in the phase noise spectrum at large offset frequencies. For the case where the processor logic is switching, these spurs are slightly larger. These spurs increase the time domain jitter and correspondingly, the measured jitter without the processor logic switching was 3.5ps and with the processor running it was 4.5ps which is approximately a 30% increase in jitter due to logic switching. These results indicate that the deep *n*-well option provides very good isolation of the oscillator core.

6.4.4 Testing Summary

All measured results are summarized in Table 6.4 and compared to simulation results were agreement is observed. Additionally, no significant performance degradation was observed between the case when the processor logic is switching and when it is not. Moreover, ultra-fast and glitch-free frequency switching was demonstrated successfully. In summary, the clock synthesizer was deployed successfully into the microsystem and clearly this synthesizer can be utilized as the sole clock reference with excellent performance.

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Performance Parameter	Simulated Value	Measured Value
Power supply rail (V)	1.8	1.8
Bias current (mA)	9.00	9.05
Power dissipation (mW)	16.20	16.29
Output frequency (MHz)	33.0	33.5
Voltage output level (high V/low V)	3.3/0	3.3/0
Duty cycle (high/low)	50/50	49.6/50.4
Phase noise PSD at 10kHz offset with no logic switching (dBc/Hz)	-92	-95.4
Phase noise PSD at 10kHz offset with logic switching (dBc/Hz)	—	-94.8
Period jitter with no logic switching (ps)	1.9	3.5
Period jitter with logic switching (ps)	—	4.5

Table 6.4   Comparison of simulated and measured performance parameters for the monolithic and top-down clock synthesizer deployed into the microsystem.

6.5 Conclusions

As the field of microsystems matures, the boundaries of system integration will continue to be challenged. The focus of future work on this microsystem will include achieving the goals of reduced power dissipation, cost and size, while realizing increased integration and functionality. A significant and unprecedented step toward reaching these goals has been presented through the development of this microsystem—a low power, compact, fully integrated microsystem in *TSMC's* 0.18μm MM/RF CMOS process. The presented design merges not only the analog and digital domains, but also the electrical and mechanical domains. The system contains a 16-bit microcontroller, a low-voltage analog front end, and a monolithic clock synthesizer, making it ideal for a variety of microinstrumentation applications, particularly micro-sensor control.

The microsystem was developed by first taking an IP-based approach to development. It was shown that IP design and reuse will become indispensable aspects of microsystem and SoC research and development in the near future. Moreover, support for analog, mixed-signal, and MEMS IP components will become commonplace as development and standardization of IP for these components matures. Through the development and use of

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IP, design cycles can be substantially reduced, and accelerated design productivity will enable more meaningful research contributions to be achieved.

An overview of microsystems technology and the trends and challenges associated with its development were presented in an effort to motivate development of an efficient top-down approach. A typical bottom-up design methodology was outlined and the associated shortcomings were addressed. By leveraging advances in mixed-signal and digital IC design tools, an efficient and effective top-down design methodology was implemented. The methodology was employed in the development of a complete microsystem. Gaps in the tool suite were presented as well as suggestions for future directions in CAD development, which has motivated the development of the tool presented in Chapter VII.

Lastly, the monolithic and top-down clock reference has been demonstrated in a microsystem application where it has been deployed as the sole clock reference for the system. Results are impressive and indicate that the developed work can indeed been utilized in microsystem, microprocessor, or microcontroller applications and replace off-chip components and the on-chip PLL or DLL. The deployment of this technology into such an application, with the results presented, truly indicates its viability.

CHAPTER VII

NEWTON: A PERFORMANCE-DRIVEN

ANALYTICAL SYNTHESIS TOOL FOR RF MEMS

THE NEED FOR MEMS device synthesis from either behavioral or topological models has been presented clearly in Chapter VI and in [132]. This becomes particularly significant when incorporating MEMS devices into large electronic systems such as the microsystem that was presented in Chapter VI [133]. In the development of such systems, designers would benefit from a tool that could provide support for the physics and manufacturing aspects of the design.

This need, however, does not come without implementation challenges. Synthesis of MEMS is not nearly as straight-forward as analogous problems in the field such as digital logic synthesis. Consider that typically MEMS devices must be modeled as continuous systems while logic can be described by a finite set of states. Also, a variety of MEMS topologies and manufacturing processes exist and every MEMS device varies substantially. Consequently, the current approach to MEMS design has been with finite element analysis (FEA), where popular tools include *Coventor* and *ANSYS*. With these FEA tools, arbitrary structures can be designed in any material and simulated for a given set of boundary conditions. Though these tools are clearly indispensable for MEMS design, their use requires substantial knowledge of MEMS device physics and manufacturing.

For the past several decades, the general trend in the area of semiconductor design has been to consider the design activity from an increasingly abstract level. For example, silicon compilers for digital logic accept HDL code from which physical design is generated. With this approach, the designer need not consider the details of the transistor level

implementation. In fact, even the gate level implementation can be bypassed by the designer using a behavioral description for the hardware under development. The advantages of this design methodology are, of course, many. First, design productivity can be increased substantially. Second, design effort can be more heavily focussed on functional and logic verification as opposed to physical design. Lastly, with the use of an APR tool, the entire physical design process can be automated. Of course, significant physical design verification effort is still required, but design iteration can be achieved in a fraction of the time required for full-custom logic and physical design.

Certainly, a similar approach could be applied to the synthesis of MEMS devices and the advantages would be similar. Bypassing the FEA would substantially increase design productivity. Similarly, some type of direct silicon compilation would reduce physical design time. Yet the question remains: with what approach and framework can these goals be attained?

It is an anomaly that FEA remains the defacto standard for MEMS design. The closest analogy that can be drawn between FEA for MEMS design and analysis for solid-state design is analysis with a semiconductor device simulator, such as *Medici* or *Davinci*. These simulators allow the designer to model a semiconductor device based on process parameters such as doping and implant concentrations. Circuit designers certainly do not simulate transistor devices at this level. In fact, a circuit designer never even considers these issues. Why, then, should a MEMS designer be concerned with similar levels of detail?

In this chapter, an alternative physics-based analytical MEMS CAD package, *Newton*, is presented. *Newton* supports direct synthesis of a physical design and an electrical model for MEMS devices from process and performance parameters. *Newton* has been shown to provide accuracy comparable to FEA while requiring a fraction of the computation time.

7.1 Overview

As just described, several implementation challenges reside in the development of a synthesis tool for MEMS. Addressing these challenges, *Newton* has been developed with a library framework. The reality of MEMS design and development is that although an infi-

nite number and variety of devices can be conceived and developed with FEA, only a finite number possess any practical use. Moreover, the numerous MEMS foundries that sprung up in the mid and late 1990's are now being consolidated and standardized [134], thus reducing the variety of available devices. This trend is again certainly not unlike the development of transistor electronics where in the early years, a variety of transistor technologies that were fabricated with a variety of manufacturing processes were promoted by commercial companies. However, now CMOS dominates the market while some heterojunction bipolar devices have found niche applications in RF and low noise electronics. Considering these trends, *Newton's* library contains previously designed components that can be selected and synthesized based on performance parameters. This finite component library is certainly not a limitation of the tool as *Newton* is an extensible software framework into which more components can be easily integrated. Components currently supported are focussed at RF devices for oscillators and include a micromechanical varactor and micromechanical resonators of two topologies: clamped-clamped beam and free-free beam.

In the sections that follow, a detailed description of the FEA approach to MEMS design is presented along with a more recent behavioral approach developed by *Coventor*. A summary of the implications associated with each design approach is presented and contrasted with the physics-based analytical approach in this work. The entire framework of *Newton* is then described, beginning with the detailed analytical descriptions for each supported component and the corresponding computational algorithms. The user interface, or front-end, is then presented and a sample synthesis problem is solved, thus further describing the tool and its use. Experimental results from devices that have been fabricated from synthesis are presented and good agreement is shown between the performance goals and the measured results.

7.2 Current Approaches

As the MEMS field has matured, so have the CAD tools for the development of MEMS. Prior to the availability of any MEMS-specific EDA tool, most early MEMS designs were developed with *ANSYS*, a general-purpose and powerful mechanical FEA tool. In recent years, a MEMS-specific FEA tool was developed and marketed under the name *MEMCAD*,

which later became *Coventorware*. This tool supported some intuitive MEMS design aspects including 3-dimensional model generation from a wafer-level fabrication process and mask set. Certainly this approach reduced the complexity involved in 3D model generation, but still, a 2D physical design was required and FEA remained the analysis and design approach. Now, within the past couple of years, a behavioral tool, based on the original *Saber* framework has been introduced by *Coventor* where the electromechanical behavioral descriptions facilitate design and drastically reduce computation complexity and the corresponding simulation time. The following two sections provide some additional detail pertaining to both early and now state-of-the-art approaches to MEMS design.

7.2.1 Finite Element Analysis

FEA is an analysis technique by which an object is dissected into a finite number elements and analyzed based on mechanical constraints, or boundary conditions, that are placed upon specific elements. The technique requires significant computation time for both finite element generation, commonly called meshing, and solution convergence. Additionally, a significant amount of design effort is required to generate a 3-dimensional representation of the structure to be simulated. An illustration of a simple beam and a brick mesh is shown in Figure 7.1. In a typical application, the beam may be fixed at one or both ends and a corresponding boundary condition is placed on the appropriate elements.

(a)   (b)
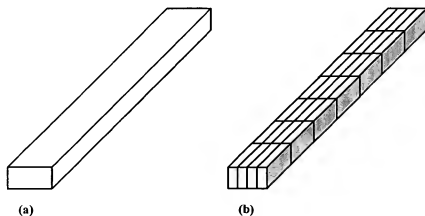
Figure 7.1   Brick mesh of a simple beam for FEA. (a) The beam. (b) The beam meshed.

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Mesh and simulation time are largely contingent upon the mesh size and type. Common mesh geometries include brick, triangular, and hexahedral geometries and the designer typically selects the most appropriate mesh element for the given geometry. Clearly, in Figure 7.1, the selection is brick. Of course, as the mesh size is reduced, the accuracy is increased, but so is the computational complexity and simulation time, and thus there is a trade-off between accuracy and complexity.

7.2.2 Behavioral Modeling

An alternative and analytical approach has been presented in [135]. The approach makes use of parameterized electromechanical models (PEM). These models comprise the foundation of the behavioral models employed in *Coventorware's ARCHITECT* tool. The behavioral models are coded in HDL using either *Saber's* proprietary language, *MAST*, or *Verilog-A*. The latter is, of course, more useful for development within IC design frameworks. These models allow the designer to link together objects within a schematic-capture framework and attach boundary conditions to the objects along any cartesian coordinate. Additional parameters are required to describe the material properties of each object. These boundary conditions and material properties comprise the parameters for the behavioral model. Using this technique, the simulation is very fast as compared to FEA. Results have been presented in [135] and [136] and show good agreement with FEA where typical error is on the order of 2% or less, although for some analyses the error has been shown to be as high as 5% for certain performance metrics.

Coventorware's ARCHITECT also supports parameterized layout generation from the netlist that is extracted from the schematic capture utility. Devices can be fabricated from the generated mask set or they can be simulated further using FEA where a solid model generator is required to transform the 2D mask set into a 3D model. This approach is certainly a significant advance in the development of MEMS EDA tools as it substantially reduces design and simulation time. However, this approach is still design-oriented as opposed to an approach based on direct synthesis of the MEMS component from a set of performance parameters. Indeed these behavioral models accept boundary condition and material parameters, not performance parameters. Thus, the user must possess knowledge

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of MEMS design in order to develop a component that converges to the performance specification desired, which requires time-consuming design iteration. A solution to this bottleneck is the parameterized analytical and direct-synthesis approach presented in this work.

7.3 A Performance-Driven, Analytical, and Direct Synthesis Approach

In this work, analytical expressions are derived and solved for the synthesis of MEMS components directly from the performance specification and process parameters to the physical design. With this approach, the costly simulation and design time associated with FEA is reduced substantially. As compared to other analytical approaches, no MEMS-specific design knowledge is required for synthesis, and convergence to a specification is achieved by *Newton*, not the designer. Lastly, in this approach, lumped-parameter equivalent circuits have been derived, which provide significant utility for co-simulation of MEMS and transistor circuitry.

Currently *Newton* supports three RF MEMS components including MEMS varactors and micromechanical resonators of two topologies: clamped-clamped beam and free-free beam. However, as will be shown, the framework can be extended easily. The details of the derived analytical and computational algorithms for the currently supported devices are described next.

7.4 Analytical Expressions and Computational Algorithms

7.4.1 Micromechanical Varactor

A generalized micromechanical parallel plate varactor was presented in Chapter IV and is shown here again in Figure 7.2, along with an equivalent lumped-parameter circuit. Performance metrics of interest to a designer include the nominal capacitance and the pull-in voltage, which together specify the tuning range and DC voltages required for operation. These parameters, along with an equivalent electrical model are derived here.

The variable capacitance realized by this structure is described by the following relationship,
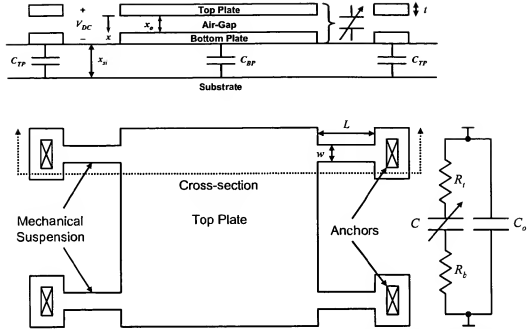
Figure 7.2   Top and cross-sectional views of a generalized micromechanical parallel-plate varactor along with equivalent electrical circuit.

$$C = \frac{\varepsilon A}{x_o - x} \tag{7.1}$$

where ε is the permittivity of air, A is the plate overlap area, x_o is the nominal distance between the plates, and x is some displacement forced by the DC tuning voltage, V_{DC}. Analytical performance expressions can be derived from the relationship in (7.1). Assuming that the plates remain flat throughout deflection, the electrostatic force, F_e, generated between the plates by the applied tuning voltage, V_{DC}, can be derived by considering the energy, E, stored between the plates.

$$F_e = \frac{\partial E}{\partial x} = \frac{1}{2}\frac{\partial C}{\partial x}V_{DC}^2 = \frac{1}{2}\frac{CV_{DC}^2}{(x_o - x)} \tag{7.2}$$

The relationship between the electrostatic force and the force created by the mechanical suspension network can be determined by first finding the electrical spring constant, k_e. By definition, it is given by the magnitude of the differential of this force with respect to displacement.

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$$k_e = \left| \frac{\partial F_e}{\partial x} \right| = \frac{C V_{DC}^2}{(x_o - x)^2} = \frac{\varepsilon A V_{DC}^2}{(x_o - x)^3} \tag{7.3}$$

A mechanical spring constant, k_m, is associated with the suspension network. A mechanical restoring force, F_m, is created by this suspension. The relationship between k_m and F_m is given by Hooke's Law.

$$F_m = k_m x \tag{7.4}$$

The expression for mechanical spring constant can be determined simply from geometry. The general expression is [105],

$$k_m = \frac{\beta E w t^3}{L^3} \tag{7.5}$$

where β depends on the support network topology. Common topologies and the corresponding values for β are shown in Figure 7.3.

The magnitudes of F_m and F_e are the same at equilibrium, as the electrostatic force is balanced by the mechanical restoring force of the suspension network.

$$k_m x = F_e = \frac{1}{2} \frac{C V_{DC}^2}{(x_o - x)} \tag{7.6}$$

Finally, the relationship between V_{DC} and x can be expressed using (7.6).

$$V_{DC} = \sqrt{\frac{2 k_m x (x_o - x)^2}{\varepsilon A}} \tag{7.7}$$

It has been shown in Chapter IV that when $x = x_o/3$, the plates will pull together. This pull-in voltage is given by,

$$V_{pull-in} = \sqrt{\frac{2 k_m (x_o/3)(x_o - x_o/3)^2}{\varepsilon A}} = \sqrt{\frac{8 k_m x_o^3}{27 \varepsilon A}} \tag{7.8}$$

The plate resistance (applied to both top and bottom) was derived and presented in Chapter IV. Assuming that the plate is square, the resistance of the top and bottom plates is,
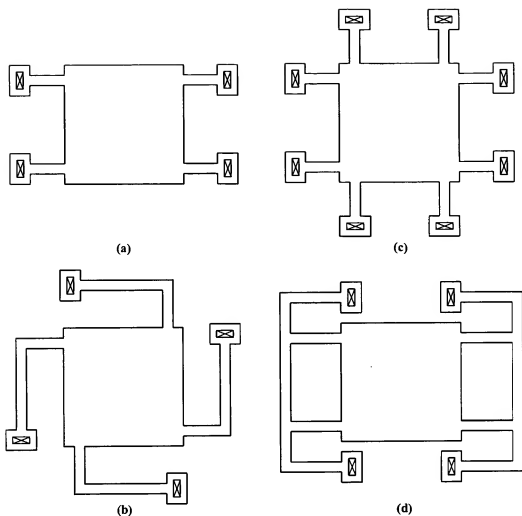
Figure 7.3   Various micromechanical varactor support topologies. (a) β = 4 (b) β = 4 (c) β = 8 (d) β=2

$$R_t = R_b = \frac{2\rho}{t} \qquad (7.9)$$

The only remaining calculations that must be made are for the parasitic top and bottom plate capacitors, which are given by,

$$C_{TP} = \frac{\eta \varepsilon A_a}{x_{si}} \text{ and } C_{BP} = \frac{\varepsilon A}{x_{si}} \qquad (7.10)$$

where η is the number of support beams, A_a is the anchor area, and x_{si} is the distance between the plane of the bottom plate and the substrate.
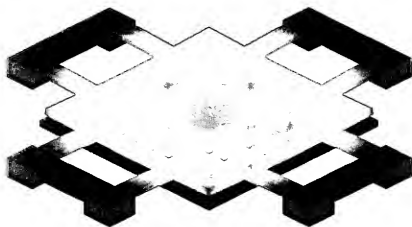
Figure 7.4 Simulation results from finite element analysis indicating curvature in the top plate displacement due to electrostatic force for a micromechanical varactor.

The only shortcoming of this analysis is that the top plate is treated as a rigid surface. In fact, the top plate bends to some extent as would be expected. An FEA simulation of this effect is shown in Figure 7.4. A more thorough analysis could certainly consider the shape of the varactor and here lies an opportunity for future work. Additional work could also be pursued in the area of more advanced support beam topologies. For example, the support beam topologies with bent arms could be rounded as opposed to at right angles, This would reduce the mechanical stress and likely prolong the lifetime of the device. However, many foundries do not support arc or circle geometries due to the increased complexity associated with mask generation. In any event, the basic varactor physics here could be easily extended to support alternative geometries.

A computational algorithm for this device is straight-forward. Performance and process variables, shown in Table 7.1, can be selected by the user and synthesis can be achieved by evaluating the expressions shown in Table 7.2. All of the relationships are algebraic and thus computation does not require use of complex numeric methods nor significant computation time. The source code that has been developed for synthesis of this part based upon these computations can be found in Appendix X, where *MATLAB*, a numeric mathematics software package, is the language utilized.

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Design Variable	Type	Description
ρ	Process	Resistivity
E	Process	Young's Modulus
t	Process	Plate and support beam thickness
x_o	Process	Distance between plates
x_{si}	Process	Bottom plate to substrate distance
C	Performance	Nominal capacitance
η	Performance	Number of support beams
$V_{pull-in}$	Performance	Pull-in voltage
A_a	Performance	Anchor area
β	Performance	Support topology
ω	Performance	Operation frequency

Table 7.1 Micromechanical RF varactor process and performance variables.

Constant/Derived Variable	Value/Expression	Description
ε	8.85×10^{-12} F/m	Permittivity of free space
Q	$Q = (\omega CR)^{-1}$	Quality factor
C_{TP} and C_{BP}	See (7.10)	Parasitic capacitance
R_t and R_b	Synthesized from (7.9)	Series resistance
w	Synthesized from (7.5) and (7.8)	Support beam width
L	Synthesized from (7.5) and (7.8)	Support beam length
A	Synthesized from (7.1)	Plate overlap area

Table 7.2 Micromechanical varactor constants and derived variables.

7.4.2 Clamped-Clamped Beam Microresonator

The clamped-clamped beam microresonator was presented in Chapter IV and is illustrated here again in Figure 7.5. It is simply comprised of a beam that is clamped at both ends and suspended over an electrode. The device is typically utilized for oscillator and filter applications and thus the most significant performance metric is the mechanical resonant frequency of the device. Two general physics-based harmonic analysis approaches can be employed to calculate the resonant frequency of this device and the corresponding lumped-

parameter electrical model. These approaches include the Euler-Bernoulli method [139] and Timoshenko's method [137], which are presented next. General purpose analytical synthesis expressions can be derived using these methods.

7.4.2.1 Euler-Bernoulli Method

For transverse vibrations of a simple beam, the mode shape equation takes the following form [34],

$$u(x) = C_1(\cos kx + \cosh kx) + C_2(\cos kx - \cosh kx) \qquad (7.11)$$

$$-C_3(-\sin kx - \sinh kx) + C_4(\sin kx - \sinh kx)$$

where C_1, C_2, C_3, and C_4 are constants; k is the wave number, and x is distance along the beam. For the clamped-clamped case, the boundary conditions are:
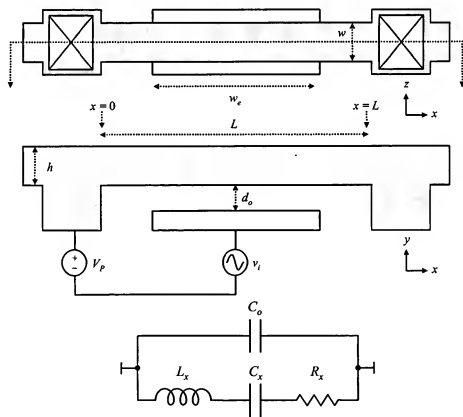
Figure 7.5   Simple top and cross-sectional illustration of a clamped-clamped beam microresonator along with equivalent lumped parameter circuit at mechanical resonance.

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$$u(0) = 0 \tag{7.12}$$

$$\left.\frac{du}{dx}\right|_{x=0} = 0 \tag{7.13}$$

$$u(L) = 0 \tag{7.14}$$

$$\left.\frac{du}{dx}\right|_{x=L} = 0 \tag{7.15}$$

The first two conditions are satisfied if $C_1 = C_3 = 0$. The remaining two conditions determine the following relationships:

$$C_2(\cos kl - \cosh kl) + C_4(\sin kl - \sinh kl) = 0 \tag{7.16}$$

$$C_2(\sin kl + \sinh kl) + C_4(-\cos kl + \cosh kl) = 0 \tag{7.17}$$

The solution to the system (7.16) and (7.17) can be determined by first evaluating the determinant.

$$(\cos kl - \cosh kl)(-\cos kl + \cosh kl) - (\sin kl - \sinh kl)(\sin kl + \sinh kl) = 0 \tag{7.18}$$

After some trivial algebra, the determinant becomes,

$$\frac{1}{\cosh kl} = \cos kl \tag{7.19}$$

There are multiple kl roots to (7.19). The first root represents the fundamental mode shape of the device. This root, and others, are pictured in Figure 7.6. Because L does not change for any of these mode shapes, it is useful to denote the wave number by k_m where m denotes the mode number. For each mode, C_1 and C_3 can be solved uniquely and thus $u(x)$ can be solved.

Recall that in Chapter II, the resonant frequency for any mechanically resonant device can be determined by solving the differential equations of simple harmonic motion. Without damping, the solution was shown to be,

$$f_o = \frac{1}{2\pi}\sqrt{\frac{k_m}{m}} \tag{7.20}$$

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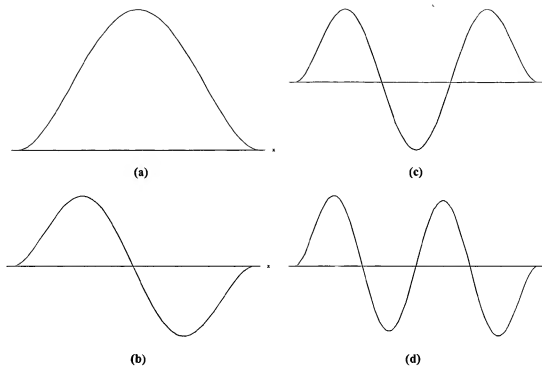
Figure 7.6 First 4 mode shapes for a clamped-clamped beam microresonator with fixed length L. (a) Fundamental mode. (b) 2nd mode. (c) 3rd mode. (d) 4th mode.

where k_m is the stiffness of the resonating body and m is its mass. In [9], it has been shown how this expression can be evaluated for the case of the clamped-clamped beam and an arbitrary mode,

$$f_n = \frac{(k_n L)^2}{2\pi L^2} \sqrt{\frac{EI}{\rho A}} \tag{7.21}$$

where E is Young's modulus, I is the moment of inertia, ρ is the density of the material, and A is wh. The moment of inertia for a prismatic beam is simply,

$$I = \frac{1}{12} w h^3 \tag{7.22}$$

and substituting yields,

$$f_n = \frac{(k_n L)^2}{2\pi \sqrt{12}} \sqrt{\frac{E}{\rho}} \frac{h}{L^2} \tag{7.23}$$

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At first glance, this expression appears to be sufficient for analytical evaluation. However, consider that the clamped-clamped beam actually experiences two spring effects: a mechanical and an electrical effect. The mechanical spring constant is determined by the stiffness of the material and the anchors. The electrical spring constant is associated with the DC voltage that is applied across the beam which effectively "softens" the spring constant associated with the system because this force is subtractive. Considering this effect, a modified version of (7.23) can be written as,

$$f_n' = \frac{1}{2\pi} \sqrt{\frac{k_m - k_e}{m}} = f_n \sqrt{1 - \frac{k_e}{k_m}} \tag{7.24}$$

$$f_n' = \frac{(k_n L)^2}{2\pi \sqrt{12}} \sqrt{\frac{E}{\rho} \frac{h}{L^2}} \left(1 - \frac{k_e}{k_m}\right)^{1/2} \tag{7.25}$$

Recall the previous analysis for the varactor where k_e can be solved by considering the energy stored between the beam and the electrode. The force can be calculated from this energy. The differential of this force with respect to displacement is the electrical spring constant. Referring to Figure 7.5, displacement is in the y direction.

$$F_e = \frac{\partial E}{\partial y} = \frac{1}{2} \frac{\partial C}{\partial y} V_p^2 = \frac{1}{2} \frac{C_o V_p^2}{d_o} \tag{7.26}$$

$$k_e = \left| \frac{\partial F_e}{\partial y} \right| = \frac{C_o V_p^2}{d_o^2} = \frac{\varepsilon A V_p^2}{d_o^3} \tag{7.27}$$

Consider that both k_m and m are functions of x, the position along the beam. Return to the general expression for the mechanical resonant frequency in (7.23) and consider the following relationship,

$$f_n = \frac{(k_n L)^2}{2\pi \sqrt{12}} \sqrt{\frac{E}{\rho} \frac{h}{L^2}} = \frac{1}{2\pi} \sqrt{\frac{k_m}{m}} \tag{7.28}$$

and solve for k_m.

$$k_m(x) = \left[\frac{(k_n L)^2 h}{\sqrt{12}L^2}\right]^2 \frac{E}{\rho}m(x) \qquad (7.29)$$

Now using (7.27) and (7.29) consider an expression for k_e/k_m over a differential length of the beam, dx, for a beam of length L. Such an expression becomes,

$$\frac{k_e}{k_m}(L)dx = \frac{V_p^2 \varepsilon w}{d_o^3} \frac{\rho L^4}{\frac{(k_n L)^4}{12}Eh^2 m(x)}dx \qquad (7.30)$$

The expression in (7.30) should be integrated over the region in which there exists a beam-electrode overlap because this is the region in which a DC bias exists across the device, thus softening the system spring constant. Assuming that the beam is positioned in x between $x = 0$ and $x = L$ and that the electrode is centered under the beam, as illustrated in Figure 7.5, (7.30) becomes,

$$\frac{k_e}{k_m}(L) = \frac{V_p^2 \varepsilon w \rho L^4}{\frac{(k_n L)^4}{12}Eh^2 d_o^3} \int_{\frac{L-w_e}{2}}^{\frac{L+w_e}{2}} \frac{1}{m(x)}dx \qquad (7.31)$$

At this point (7.31) could be evaluated by integration, except that no expression for $m(x)$ has been determined yet. This expression is determined next using a generalized equivalent mass technique [138].

The kinetic energy, KE, for any body in motion is given by,

$$KE = \frac{1}{2}mv^2 \qquad (7.32)$$

where v is the velocity of the mass. If the equivalent mass of the body varies along the position of the body, then so must the equivalent velocity, such that energy is conserved. Thus, (7.32) can be rewritten as an integral in the form,

$$m_{eq}(x) = \frac{KE}{\frac{1}{2}v^2(x)} = \frac{\frac{1}{2}\rho A}{\frac{1}{2}v^2(x)} \int_0^L v^2(x)dx \qquad (7.33)$$

Of course velocity is simply the differential of position. Thus for an object at resonance, the velocity can be described in phasor form by,

$$v(x) = j\omega u(x) \qquad (7.34)$$

where ω is the radian resonant frequency and $u(x)$ is the displacement of the beam in the y direction at position x. Now (7.33) can be rewritten with (7.34),

$$m_{eq}(x) = \frac{\frac{1}{2}\rho A \int_0^L [j\omega u(x)]^2 dx}{\frac{1}{2}[j\omega u(x)]^2} = \frac{\rho A}{u^2(x)} \int_0^L u^2(x)dx \qquad (7.35)$$

Now with an expression for $m_{eq}(x)$, an expression for $k_e/k_m(L)$ can been determined,

$$\frac{k_e}{k_m}(L) = \frac{V_p^2 \varepsilon w \not{b}}{\frac{(k_n L)^4}{12} E h^2 d_o^3} \left(\int_{\frac{L-w_s}{2}}^{\frac{L+w_s}{2}} \left(\frac{\rho A}{u^2(x)} \int_0^L u^2(x)dx \right) dx \right)^{-1} \qquad (7.36)$$

and finally (7.25) can be determined with (7.36),

$$f_n' = \frac{(k_n L)^2}{2\pi\sqrt{12}} \sqrt{\frac{E}{\rho}} \frac{h}{L^2} \left(1 - \frac{V_p^2 \varepsilon w \not{b}}{\frac{(k_n L)^4}{12} E h^2 d_o^3} \int_{\frac{L-w_s}{2}}^{\frac{L+w_s}{2}} \left(\frac{\rho A}{u^2(x)} \int_0^L u^2(x)dx \right)^{-1} dx \right)^{1/2} \qquad (7.37)$$

Thus an accurate physics-based analytical expression for the resonant frequency of the device has been determined. Moreover, the effect of spring softening on the resonant frequency of the device has been included.

In a typical application, E, ρ, d_o, and h are determined by the fabrication process. A, k_m, f_o, V_p, w_e, and W are determined by design and ε and π are a constants. Thus L can be synthesized from the design parameters using a numeric integration technique for solving (7.37) in L.

The remaining challenges reside in calculating an electrical equivalent circuit at resonance for this device. First, the series resistance is determined. Consider the schematic of a simple variable capacitor presented in Figure 7.7. The schematic models the normal behavior of the device at resonance. Let $C(t)$ represent the sum of the nominal capacitance due to the gap, C_o, and the motional capacitance, $C_m(t)$, as given by,

$$C(t) = C_o + C_m(t) \tag{7.38}$$

The total current (feed-through and motional), $i(t)$ is given by,

$$i(t) = C(t)\frac{\partial}{\partial t}v(t) + v(t)\frac{\partial}{\partial t}C(t) \tag{7.39}$$

The expression in (7.39) can be expanded by using the following relationships,

$$\frac{\partial}{\partial t}C(t) = \frac{\partial}{\partial t}C(y, t)\frac{\partial y}{\partial t} \text{ and } C_m(t) = y(t)\frac{\partial}{\partial y}C(y, t) \tag{7.40}$$

Thus, after some simplification, (7.39) becomes,
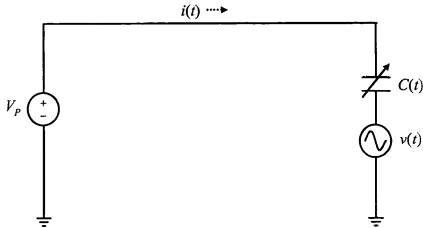
Figure 7.7 Simplified schematic modeling microresonator at resonance as a variable capacitance with applied DC and AC voltages.

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$$i(t) = C_o \frac{\mathrm{d}}{\mathrm{d}t}v(t) + y(t)\frac{\partial}{\partial y}C(y,t)\frac{\mathrm{d}}{\mathrm{d}t}v(t) - V_P\frac{\partial}{\partial y}C(y,t)\frac{\partial y}{\partial t} + v(t)\frac{\partial}{\partial y}C(y,t)\frac{\partial y}{\partial t} \qquad (7.41)$$

This expression can be written in phasor form as,

$$I(j\omega) = C_o j\omega V(j\omega) + 2\frac{\partial}{\partial y}C(y,t)j\omega V(j\omega) Y(j\omega) - V_P\frac{\partial}{\partial y}C(y,t)j\omega Y(j\omega) \qquad (7.42)$$

Only the third term represents the motional current in (7.42). The first two terms represent a feed-through signal and a double frequency signal respectively. Thus, an expression can be written for the motional current $I_m(j\omega)$,

$$I_m(j\omega) = -V_P\frac{\partial}{\partial y}C(y,t)j\omega Y(j\omega) \qquad (7.43)$$

Now the motional resistance can be determined,

$$R_x(j\omega) = \frac{V(j\omega)}{I_m(j\omega)} = \frac{1}{-V_P\frac{\partial}{\partial y}C(y,t)j\omega}\frac{V(j\omega)}{Y(j\omega)} = \frac{1}{-V_P\frac{\partial}{\partial y}C(y,t)j\omega}\frac{F(j\omega)}{Y(j\omega)}\frac{V(j\omega)}{F(j\omega)} \qquad (7.44)$$

where $F(j\omega)$ is the drive force, which is yet to be determined. From (7.44), the ratio of drive voltage to force can be shown to be,

$$\frac{V(j\omega)}{F(j\omega)} = \left[-V_P\frac{\partial}{\partial y}C(y,t)\right]^{-1} \qquad (7.45)$$

and the ratio of force to displacement is given by the generalized harmonic transfer function presented in Chapter II,

$$\frac{F(j\omega)}{Y(j\omega)} = \frac{1 - (\omega/\omega_o)^2 + j(\omega/Q\omega_o)}{k_r^{-1}} \qquad (7.46)$$

where k_r is the system spring constant, as opposed to either the mechanical or electrical spring constant alone. At resonance, (7.46) becomes,

$$\frac{F(j\omega)}{Y(j\omega)} = \frac{jk_r}{Q} \qquad (7.47)$$

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Now the ratio of drive voltage to displacement can be solved,

$$\frac{V(j\omega)}{Y(j\omega)} = \frac{F(j\omega)V(j\omega)}{Y(j\omega)F(j\omega)} = \frac{jk_r}{-QV_p\frac{\partial}{\partial y}C(y, t)} \tag{7.48}$$

and the magnitude of the motional resistance at resonance can be found from,

$$|R_x(j\omega)| = \left| \frac{k_r}{QV_p^2\left(\frac{\partial}{\partial y}C(y, t)\right)^2 \omega} \right| \tag{7.49}$$

Unfortunately the solution is not this simple, because the system spring constant, k_r, varies with position, x, along the beam. Using the equivalent mass technique presented previously define $k_m(x)$ as,

$$k_m(x) = \left[\frac{(k_n L)^2 h}{\sqrt{12}L^2}\right]^2 \frac{E}{\rho} m_{eq}(x) \tag{7.50}$$

where $m_{eq}(x)$ is as defined in (7.35). Then subtract the electrical spring constant to attain $k_r(x)$.

$$k_r(x) = k_m(x) - k_e \tag{7.51}$$

$Y(j\omega)$ also varies with x because the beam does not deflect by the same amount in every place. Thus consider (7.48) again, but in the form,

$$Y(j\omega, x) = \frac{-QV_p\frac{\partial}{\partial y}C(y, t)}{jk_r(x)V(j\omega)} \tag{7.52}$$

The expression in (7.52) can be evaluated by considering a differential distance along the beam in the x direction. The deflection caused by the force and in the specific mode shape can be determined by integrating this differential over the electrode and normalizing by the mode shape. Thus, (7.52) becomes,

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$$Y(j\omega, x) = \frac{V_p Q \varepsilon w u(x)}{V(j\omega) d_o^2} \int\limits_{\frac{L-w_e}{2}}^{\frac{L+w_e}{2}} \frac{1}{u(x) k_r(x)} dx \tag{7.53}$$

Now that Y has been determined, its variation with x can also be found by integration of a differential length along the beam.

$$I(j\omega) = \frac{\omega V_p \varepsilon w}{d_o^2} \int\limits_{\frac{L-w_e}{2}}^{\frac{L+w_e}{2}} Y(x) dx \tag{7.54}$$

The final analytical expression for the motional resistance is given by,

$$|R_x| = \left| \frac{V(j\omega)}{I(j\omega)} \right| = \frac{\omega V_p^2 Q \varepsilon^2 w^2}{d_o^4} \int\limits_{\frac{L-w_e}{2}}^{\frac{L+w_e}{2}} u(x) \left(\int\limits_{\frac{L-w_e}{2}}^{\frac{L+w_e}{2}} \frac{1}{u(x) k_r(x)} \right) dx \tag{7.55}$$

The remaining circuit parameters are, by comparison, simple to determine. One such technique has been presented in [9] and [139]. However, a simpler approach is to back out the expression for the inductance from the expression for Q-factor.

$$Q = \frac{\omega L_x}{R_x} \text{ and } L_x = \frac{R_x Q}{\omega} \tag{7.56}$$

and then determine the capacitance from the resonant frequency.

$$\omega = \sqrt{\frac{1}{L_x C_x}} \text{ and } C_x = \frac{1}{\omega^2 L_x} \tag{7.57}$$

Lastly, the nominal overlap capacitance is simply given by geometric analysis,

$$C_o = \frac{\varepsilon w w_e}{d_o} \tag{7.58}$$

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Design Variable	Type	Description
ρ	Process	Density
E	Process	Young's Modulus
h	Process	Beam height
d_o	Process	Beam to electrode distance
k_n	Performance	Determined by mode
V_p	Performance	Bias voltage
w	Performance	Beam width
w_e	Performance	Electrode width
Q	Performance	Estimated Q
f_o	Performance	Resonant frequency

Table 7.3 Clamped-clamped beam process and performance variables for the Euler-Bernoulli method.

The expressions in (7.55), (7.56), (7.57), and (7.58) can be determined directly from process and performance parameters. Table 7.3 summarizes these parameters, while a summary of constants, defined variables, and synthesis variables is presented in Table 7.4. The solution to these expressions and the solution to (7.37) are determined in *Newton* using

Constant/Derived Variable	Value/Expression	Description
ε	8.85×10^{-12} F/m	Permittivity of free space
A	$A = wh$	Beam cross-sectional area
I	Defined by (7.22)	Moment of inertia
$u(x)$	Defined by (7.11)	Mode shape eigenfunction
L	Synthesized from (7.37)	Beam length
R_x	Calculated from (7.55)	Resistance, lumped parameter equivalent circuit
L_x	Calculated from (7.56)	Inductance, lumped parameter equivalent circuit
C_x	Calculated from (7.57)	Capacitance, lumped parameter equivalent circuit
C_o	Calculated from (7.58)	Overlap capacitance, lumped parameter equivalent circuit

Table 7.4 Clamped-clamped beam constants, defined, and derived variables for the Euler-Bernoulli method.

Mathematica, a symbolic mathematics package. *Mathematica* was selected due to the fact that it supports symbolic integration, which appears often in this analysis. A listing of the code is included in Appendix X. The algorithm involves using the design and process parameters in order to synthesize the device length, L, based upon convergence to the correct root of (7.37). The remaining parameters are simply calculated from the respective definitions.

7.4.2.2 Timoshenko's Method

Timoshenko's method involves the solution of two differential equations as shown in [137]. The method has been shown to me more accurate than the Euler-Bernoulli method because shearing and rotatory inertia are considered [139]. These equations are not presented here, but the solution to this system results in the following two eigenfunctions,

$$\phi(x) = C_1 \cosh\frac{\alpha x}{L} + C_2 \sinh\frac{\alpha x}{L} + C_3 \cos\frac{\beta x}{L} + C_4 \sin\frac{\beta x}{L} \tag{7.59}$$

$$\psi(x) = \frac{\frac{p^2 E}{\kappa G} + \alpha^2}{\alpha L}\left(C_2\cosh\frac{\alpha x}{L} + C_1\sinh\frac{\alpha x}{L}\right) + \frac{\frac{p^2 E}{\kappa G} - \beta^2}{\beta L}\left(C_3\sin\frac{\beta x}{L} + -C_4\sinh\frac{\beta x}{L}\right) \tag{7.60}$$

where,

$$p^2 = \frac{\omega^2 L^2 E}{\rho} \tag{7.61}$$

$$\begin{bmatrix} \alpha^2 \\ \beta^2 \end{bmatrix} = \frac{p^2}{2}\left[\mp\left(1 + \frac{E}{\kappa G}\right) + \sqrt{\left(1 - \frac{E}{\kappa G}\right)^2 + \frac{4L^2}{p^2 r^2}}\right] \tag{7.62}$$

These eigenfunctions are valid for a resonant beam with any boundary condition. For the case of the clamped-clamped beam, the boundary conditions depend on the mode. Assume that the beam is centered around the point $x = 0$ (which differs from the origin in the Euler-Bernoulli method presented previously). For symmetric, or odd modes, the boundary conditions are as follows.

$$\left.\frac{d\phi}{dx}\right|_{x=0} - \psi(0) = 0 \tag{7.63}$$

$$\psi(0) = 0 \tag{7.64}$$

$$\phi\left(\frac{L}{2}\right) = 0 \tag{7.65}$$

$$\psi\left(\frac{L}{2}\right) = 0 \tag{7.66}$$

Using these boundary conditions, the system of equations shown in (7.59) and (7.60) can be solved, the significance of which includes an expression for the mode shape and a corresponding frequency equation given by [137],

$$\tan\left(\frac{\beta}{2}\right) + \frac{\beta}{\alpha}\left(\frac{\alpha^2 + p^2\kappa G/E}{\beta^2 - p^2\kappa G/E}\right)\tanh\frac{\alpha}{2} = 0 \tag{7.67}$$

For antimetric modes, the boundary conditions at $x = 0$ are different than for the symmetric case. They are,

$$\phi(0) = 0 \tag{7.68}$$

$$\left.\frac{d\psi}{dx}\right|_{x=0} = 0 \tag{7.69}$$

and the corresponding frequency equation is [137],

$$\tan\left(\frac{\beta}{2}\right) - \frac{\alpha}{\beta}\left(\frac{\beta^2 - p^2\kappa G/E}{\alpha^2 + p^2\kappa G/E}\right)\tanh\frac{\alpha}{2} = 0 \tag{7.70}$$

As would be expected, both frequency equations are periodic in L. The symmetric frequency equation is plotted against L in Figure 7.8. The trivial solution does not represent a resonant mode. However, each solution from that point and for increasing positive L corresponds to a resonant mode. Synthesis can be achieved by convergence to the appropriate solution for L given a distinct mode and a set of process and performance parameters. The
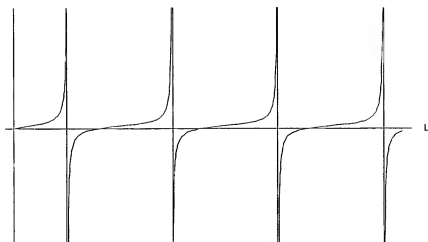
Figure 7.8 Timoshenko's symmetric frequency expression as a function of L. Each zero-crossing represents a solution to (7.70). Each solution beyond the trivial solution represents a corresponding mode.

parameters associated with this analytical method are listed in Table 7.5. The corresponding constants, defined, and derived expressions are presented in Table 7.6.

With the appropriate set of boundary conditions, which is based upon the mode selected, the mode shape equation can be solved. This mode shape equation can be used in place of the mode shape equation used for the Euler-Bernoulli method and the motional

Design Variable	Type	Description
ρ	Process	Density
E	Process	Young's Modulus
ν	Process	Poisson's ratio
h	Process	Beam height
d_o	Process	Beam to electrode distance
m	Design	Mode
w	Design	Beam width
w_e	Design	Electrode width
V_p	Design	Bias voltage
f_o	Design	Resonant frequency

Table 7.5 Clamped-clamped beam process and design variables for Timoshenko's method.

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Constant/Derived Variable	Value/Expression	Description
ε	8.85×10^{-12} F/m	Permittivity of free space
κ	2/3	Shape factor
A	$A = wh$	Beam cross-sectional area
I	$wh^3/12$	Moment of inertia
r^2	I/A	Ratio of inertia to area
G	$G = E/(2 + 2\upsilon)$	Shearing modulus
c_o	$c_o = \sqrt{E/\rho}$	Acoustic velocity
p	Defined by (7.61)	Intermediate variable
α	Defined by (7.62)	Intermediate variable
β	Defined by (7.62)	Intermediate variable
ϕ	Defined by (7.59)	Mode shape eigenfunction
ψ	Defined by (7.60)	Shearing eigenfunction
L	Synthesized from (7.70)	Beam length
R_x	Calculated from (7.55)	Resistance, lumped parameter equivalent circuit using $\phi(x)$ in place of $u(x)$
L_x	Calculated from (7.56)	Inductance, lumped parameter equivalent circuit
C_x	Calculated from (7.57)	Capacitance, lumped parameter equivalent circuit
C_o	Calculated from (7.58)	Overlap capacitance, lumped parameter equivalent circuit

Table 7.6 Clamped-clamped beam constants, defined, and derived variables for Timoshenko's method.

resistance can be determined using the same expressions presented previously. The remainder of the lumped parameter electrical circuit can also be solved in exactly the same manner as presented previously.

7.4.3 Free-Free Beam Microresonator

A free-free beam microresonator is a device that is free at both ends and is thus virtually levitated. The first four mode shapes for a device with these boundary conditions is shown in Figure 7.8. Here it is important to observe that there are nodal points associated with each
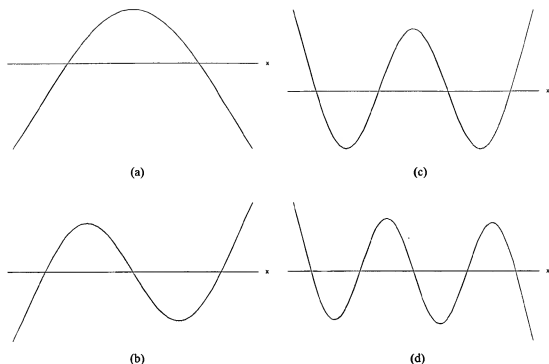
Figure 7.9   First four mode shapes for a free-free beam microresonator. (a) Fundamental mode. (b) 2nd mode. (c) 3rd mode. (d) 4th mode.

mode shape that are not at the ends of the beam. At these points, no vertical displacement occurs, but rather torsional displacement. This fact is exploited in order to virtually levitate the device with presenting vertical translation impedance.

A simple illustration of a free-free beam microresonator is shown in Figure 7.10. The beam body is effectively levitated by support beams that are positioned at the nodal points of vertical deflection. Figure 7.11 illustrates the mechanical deflection at these points. Clearly there is no vertical deflection, but rather the support beam experiences torsional rotation. Thus synthesis must include first, the length of the free-free beam based upon lateral mode resonance and second, the length of the supports based upon torsional mode resonance. The torsional resonance problem must be solved such that an effective impedance transformation is achieved. Specifically, the infinite mechanical impedance at the anchor must be transformed into a zero torsional impedance at the end of the support beam, which is connected to the free-free beam. Again, two approaches can be employed and many of the results from the clamped-clamped analysis can be utilized.

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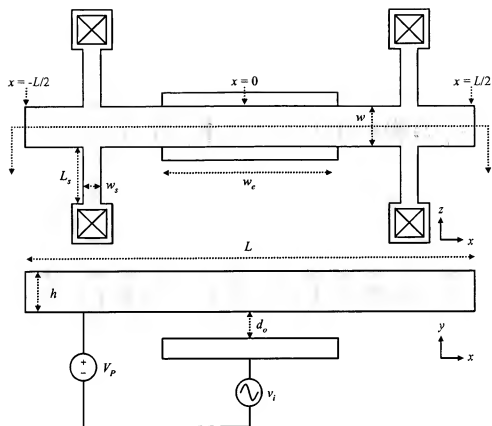
Figure 7.10   Simple top and cross-sectional illustration of a fundamental mode free-free beam microresonator. The support beams are positioned at the nodal points of vertical deflection.
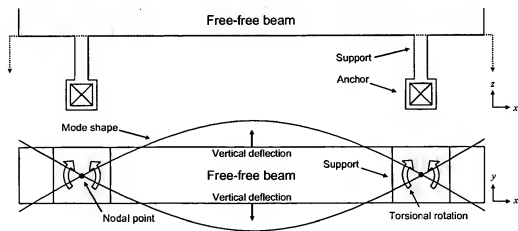
Figure 7.11   Cross-sectional view of free-free beam illustrating torsional rotation of support beams at the nodal points of the mode shape.

7.4.3.1 Euler-Bernoulli Method

The Euler-Bernoulli method for the free-free beam is identical to the clamped-clamped case except that the mode shape must be derived again. The boundary conditions for the free-free case are,

$$\frac{d^2 u}{dx^2}\bigg|_{x=0} = 0 \tag{7.71}$$

$$\frac{d^3 u}{dx^3}\bigg|_{x=0} = 0 \tag{7.72}$$

$$\frac{d^2 u}{dx^2}\bigg|_{x=L} = 0 \tag{7.73}$$

$$\frac{d^3 u}{dx^3}\bigg|_{x=L} = 0 \tag{7.74}$$

The first two conditions can be satisfied when $C_2 = C_4 = 0$. The remaining two conditions yield the following two expressions:

$$C_1(-\cos kl + \cosh kl) + C_3(-\sin kl + \sinh kl) = 0 \tag{7.75}$$

$$C_1(\sin kl + \sinh kl) + C_3(-\cos kl + \cosh kl) = 0 \tag{7.76}$$

Non-zero solutions exist for the system of (7.75) and (7.77) when the determinant of the coefficients is zero.

$$(-\cos kl + \cosh kl)^2 - (\sin kl)^2 + (\sinh kl)^2 = 0 \tag{7.77}$$

Using trigonometric identities, (7.77) can be reduced to,

$$\cos kl \cosh kl = 1 \tag{7.78}$$

The roots in (7.78) are different than those for the clamped-clamped case as presented in (7.19). Again, each root corresponds to a particular mode shape. Also, for each

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root, C_2 and C_4 can be solved uniquely as shown in the clamped-clamped beam analysis. The resonant frequency of the device can then be derived in exactly the same manner as shown in clamped-clamped beam analysis. In fact the only difference in the analyses is the fact that the mode shape equations are different. The process and design parameters are identical for both cases, as are the equations for synthesis. However, additional analysis is required in order to synthesize the geometry for the support beam.

In order to effectively levitate the free-free beam, a motional impedance transformation is required. Consider a supporting beam that is connected to one of the mode shape nodal points of the device. The support beam will experience only torsional rotation at this node. Thus, the support beam must anchor to the substrate at one point and present zero torsional impedance to the resonant beam. Figure 7.11 illustrates this concept.

The solution to this problem has been presented in [139] and only the results are shown here. In order to meet the requirements just described, the beam length must be,

$$L_s = \frac{1}{4f_o} \sqrt{\frac{12G\gamma w^2}{\rho(h^2 + w^2)}}$$

(7.79)

or any quarter-wavelength multiple of this length based upon the wavelength of the resonant frequency. The expression in (7.79) was determined using an acoustic impedance transformation technique based upon quarter-wavelength matching.

All of the analytical expressions required for synthesis are now derived. Synthesis is achieved in a manner identical to the technique used in the clamped-clamped beam synthesis program. Process and performance parameters are selected and L can be synthesized using the equivalent mass technique shown previously where the only difference between the analyses is that the mode shape equation is specific to each device topology. The support beam length is synthesized from the algebraic expression in (7.79). The support beam locations are synthesized from by solving the locations at which the mode shape equation is equal to zero. Lastly, the equivalent lumped parameter electrical circuit can be derived in a manner identical to the clamped-clamped case, except with the use of the mode shape equation for the free-free beam. A complete listing of the code for synthesis of this device is listed in Appendix X.

7.4.3.2 Timoshenko's Method

The Timoshenko method for the free-free beam structure takes an identical approach as the clamped-clamped beam approach. Here again, the only significant differences between the two analyses are the mode shape and the corresponding frequency equation.

The boundary conditions for the free-free case are the same as for the clamped-clamped case at $x = 0$ for both the symmetric and antimetric modes. At $x = L/2$ the boundary conditions are different for the free-free case, but identical for both modes. They are,

$$\left. \frac{d\phi}{dx} \right|_{x = \frac{L}{2}} - \psi\left(\frac{L}{2}\right) = 0 \tag{7.80}$$

$$\left. \frac{d\psi}{dx} \right|_{x = \frac{L}{2}} = 0 \tag{7.81}$$

Again the system of equations shown in (7.59) and (7.60) can be solved using these boundary conditions. The corresponding frequency equation for the antimetric modes is,

$$\tan\left(\frac{\beta}{2}\right) - \frac{\alpha}{\beta}\left(\frac{\beta^2 - p^2}{\alpha^2 + p^2}\right)\tanh\frac{\alpha}{2} \tag{7.82}$$

and for the symmetric modes,

$$\tan\left(\frac{\beta}{2}\right) + \frac{\beta}{\alpha}\left(\frac{\alpha^2 + p^2}{\beta^2 - p^2}\right)\tanh\frac{\alpha}{2} \tag{7.83}$$

The analytical expressions are all that is required for synthesis. The beam length can be synthesized using (7.82) or (7.83), depending on the mode. The mode shape equation, given by (7.59), can be solved using the boundary conditions in (7.80) and (7.81). The nodal points along the beam can be determined by solving for the positions at which the mode shape equation is equal to zero. Also, the motional resistance can be determined from (7.55), where the Timoshenko mode shape expression, $\phi(x)$, is used in place of the Euler-Bernoulli expression, $u(x)$. The support beam length can be determined again from (7.79)

and the remaining parameters of the equivalent lumped parameter circuit can be determined as shown previously.

7.5 Tool Framework

Newton is partitioned into a graphical user interface (GUI)[1] and a synthesis engine in order to facilitate the development and addition of new devices to the library. The tool has a uniform GUI shared by all components and an individual synthesis scripts for each component. The interaction between the GUI and the synthesis engine is illustrated in Figure 7.12. To add a new component, one need only add a new component script to the engine. This modularity greatly facilitates the ability to expand the capabilities of the tool.

The synthesis engine is comprised of the synthesis scripts which have been coded based upon the analysis presented in the previous sections. User interaction with the GUI can be described in two phases. Referring to Figure 7.13, in the first phase the user selects
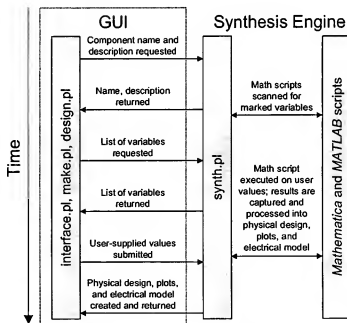
Figure 7.12 The *Newton* framework partitioned into a GUI and a synthesis engine. The chronology of steps involved with a typical synthesis procedure is indicated by the time axis.

1. The GUI described in this work was developed by James L. McCann.

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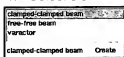
1. Select Device

2. Enter Material and Performance Parameters
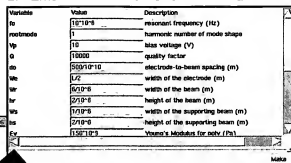
3. Verify Solution and Mode Shape
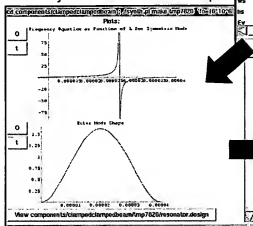
4. View and Edit Physical Design
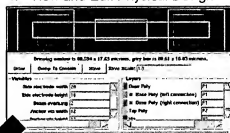
5. Output to CIF and SPICE Files

Figure 7.13 Initiating synthesis with the GUI to *Newton*. First, a device is selected from the component library browser. Component-specific material and performance parameters are entered next. The solution and mode shape are then viewed for synthesis verification.

a device from the library browser and specifies the performance and process-dependent parameters within the component parameter interface. Then synthesis is initiated. Results can be verified by examining the frequency equation graph and the mode shape as shown in Figure 7.13. In the second phase, the user is presented with a graphical display of the mask set for the component and allowed to adjust those parameters that are not fixed by the desired performance characteristics. These include options such as interconnect positions and electrode size for a resonator. Once the design is complete, the user may export both a physical layout in CIF for fabrication and electrical model of the component in SPICE format for simulation with other MEMS devices or transistors.

7.5.1 Graphical User Interface

Perl and the GUI package Perl/Tk were utilized to develop *Newton*'s GUI since these packages are easily portable across operating environments and allow for rapid software devel-

opment. The partition of *Newton*, however, allows new MEMS library component synthesis scripts to be written in any programming language. In this work, *Newton* was compiled for the *SUN Solaris* operating environment. The results and illustrations that follow are based upon use of the tool within this environment.

7.5.2 Synthesis Engine

Synthesis scripts have been developed with *Mathematica* and *Matlab* but could be eventually coded directly into the design framework with the aid of a math package. This would eliminate the need for licenses for these packages. However, the synthesis scripts were developed with these tools due to the mostly symbolic nature of the analytical expressions derived in the previous sections. Some challenges reside in porting the code for these analytical expressions to the code supported by a numeric math package, particularly in instances where intermediate symbolic solutions must be replaced with numeric solutions. For these reasons, this activity was not pursued in this work.

7.6 A Synthesis Example

As a benchmark and synthesis example, a 10MHz polysilicon clamped-clamped beam micromachined resonator was synthesized with *Newton* using Timoshenko's method. The procedure and data from this design example are exactly those shown in Figure 7.13. First, the clamped-clamped beam library part is selected from the library component browser. The process and performance parameters are entered into the synthesis form; the values for this example are listed for the reader's convenience in Table 7.7. Synthesis is initiated by selecting the *make* button. The frequency equation is plotted against L and displayed along with the mode shape equation. In Figure 7.13, it can be seen that indeed the synthesis script has converged to the first nontrivial solution of the frequency equation and that the mode shape corresponds to the first resonant mode. Once design convergence has been verified, the physical design can be edited in real time. The physical design is generated automatically and displayed within a form where attributes that do not affect performance can be modified. For example, the amount by which the beam overhangs the anchor on each side can be modified. These parameters were adjusted appropriately and the design was

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Process Parameter	Value	Design Parameter	Value
Resonator height, h	6µm	Resonant frequency, f_o	10MHz
Beam-electrode gap, d_o	1000Å	Mode, m	1
Density, ρ	2330kg/m^3	Resonator width, w	6µm
Young's modulus, E	150GPa	Electrode width, w_e	$L/2$
Poisson's ratio, v	0.29	Bias voltage, V_p	10V

Table 7.7 Summary of clamped-clamped beam process and performance parameters for synthesis of a 10MHz resonator using Timoshenko's method.
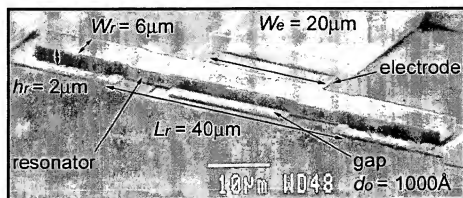
Figure 7.14 Electron micrograph of a fabricated surface micromachined 10MHz clamped-clamped beam resonator in polysilicon.

exported to CIF for mask generation. The device was fabricated using a custom polysilicon surface micromachining process in the University of Michigan's Solid State Electronic Laboratory. An electron micrograph of fabricated device is shown in Figure 7.14[2].

7.7 Experimental Results

Prior to testing the fabricated device, the physical design from *Newton* was imported into the FEA tool *Coventorware*. An accurate 3D model was generated from process parameters that corresponded to the fabrication process for the device. A brick mesh of the 3D device was created and harmonic analysis was performed. The simulated fundamental mode resonant frequency was 10.86MHz.

2. Device fabrication by Michael S. McCorquodale, Ark-Chew Wong, Mustafa Demirci, and Yuan Xie.
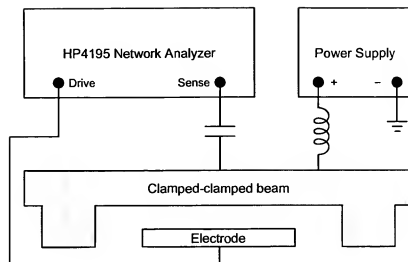
Figure 7.15 Test set-up for measuring S_{21} of clamped-clamped beam resonator in order to determine resonant frequency.

The resonant frequency of the fabricated clamped-clamped beam device was determined by measuring S_{21} with an HP4195 network analyzer. The device under test was placed under a vacuum pressure of approximately 100mTorr. The test configuration is illustrated in Figure 7.15. Here a DC bias is applied to the beam of the device through an RF choke, which limits AC coupling into the power supply. The network analyzer drives the electrode with a swept AC signal centered at the ground potential. The current that is induced by deflection of the beam is AC coupled through a capacitor and back to the net-
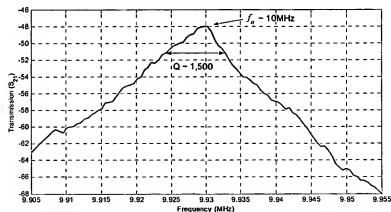
Figure 7.16 S_{21} plot of 10MHz surface micromachined polysilicon resonator acquired with an HP4195 vector network analyzer. The measured quality factor is approximately 1,500.

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work analyzer. The measured spectrum in shown in Figure 7.16, where the resonant frequency is 9.93MHz and the quality factor is approximately 1,500.

Results from both *Newton* and *Coventorware* are close to the measured resonant frequency for the device. The simulated resonant frequency within *Coventorware* was 8.6% in error as compared to fabricated devices while the *Newton* design was in error by only 0.7%. Accuracy differences between the two packages likely arises from the fact that the synthesis scripts in *Newton* account for electrical frequency pulling, while the modal analysis in *Coventorware* is a mechanical analysis that does not take this phenomenon into account.

All of the remaining devices *Newton*'s component library have been synthesized, fabricated, and tested. Results are not presented here in the interest of space. Rather, the performance of the clamped-clamped beam is reported here as typical performance for the tool.

7.8 Conclusion

Newton is the first EDA tool that supports physics-based analytical synthesis of MEMS components from a performance specification directly to physical design, while also including an equivalent lumped-parameter electrical model for mixed-mode simulation with transistors or other MEMS components. *Newton* has been shown to be a fast and accurate tool for the design of MEMS components. As a benchmark, a 10MHz polysilicon clamped-clamped beam micromachined resonator was synthesized with *Newton* and the measured resonant frequency was in error by only 0.7%.

Newton could certainly be developed into a much more substantial tool through expansion of the component library. Each part would require analytical analysis and derivation of critical performance parameters. The developed analytical expressions would then need to be coded into some math package, such as those used here. Synthesis accuracy could then be determined through fabrication and test.

Beyond expanding the component library, the tool could be developed to increase automation. For example, currently the user must enter process-dependent parameters. As

MEMS foundries standardize, this aspect of the design flow could be eliminated. The user could simply select the appropriate foundry from a list and the process-dependent parameters would be set accordingly. Certainly many other similar developments could be investigated as the field of MEMS design automation matures.

CHAPTER VIII

CONCLUSION AND FUTURE DIRECTIONS

THE TECHNICAL CONTRIBUTIONS and achievements of this work are described within this chapter.

8.1 Technology Related Achievements

A new top-down systemic approach to clock synthesis has been introduced in this work. With this approach, low jitter clock synthesis can be achieved with a monolithic and harmonic electrical reference that is of reasonable size on a silicon substrate. In fact, it has been shown that the jitter of a system where the top-down synthesis approach is utilized can equal, if not be less than, the jitter attained with a crystal-based clock synthesizer. In applications where the clock synthesizer multiplication factor is on the order of 50 or higher, the developed synthesis approach is typically superior. It was shown that such a multiplication factor is quite common in commercial applications.

In the development of the harmonic reference utilized in this work, a CMOS-compatible RF MEMS process was introduced. Both M5-M6 varactors and suspended inductors were fabricated successfully using this process. However, the MiM varactors were not operational due to an inability to etch the dielectric material that defines the gap between these devices. It was determined that M5-M6 varactors, though operational, required an unreasonable amount of silicon area for this application. Consequently, the varactor tuning approach was abandoned while the inductor suspension technique was pursued. In light of this engineering set-back, an alternative, and also systemic, frequency tuning approach was introduced. In this approach, the oscillation frequency is tuned by modulating the frequency-pulling factor, α.

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Theoretical expressions for all critical metrics were derived including phase noise, jitter, temperature stability, bias stability, and tuning range. Very good agreement was found between measured data and predicted results. Additionally, the measured performance of the developed clock synthesizer was outstanding over all of the metrics just described.

A modified rendition of the clock synthesizer demonstrated in Chapter V was also developed into a microsystem in order to verify that it could serve as the sole clock reference for such a system without performance degradation and without any external reference. In this application, frequencies from 2kHz to 1.1GHz were synthesized, where the maximum utilized frequency was 132MHz. It was shown that the deep n-well process option provided good isolation of the clock synthesizer and performance was impacted negligibly by the switching of the nearby processor logic. Additionally, it was shown that the microsystem could boot-up from the clock synthesizer with no external components and execute millions of instructions without error. Lastly, ultra-fast and glitch-free frequency switching was demonstrated as yet another architectural benefit of the developed synthesis approach.

Throughout the development of the clock synthesizer into the microsystem, several integrated circuit design issues were addressed. An IP-based design methodology was introduced and employed at the top-level. The detailed design effort involved a top-down methodology, as was shown in Chapter VI. Throughout this development effort, gaps in the design tool suite were identified, one of which was synthesis of MEMS from a behavioral or performance specification. Consequently, in Chapter VII, *Newton* was developed and introduced. *Newton* is a physics-based RF MEMS synthesis tool that has been demonstrated with very good performance as compared to measured results.

In all, contributions contained within this work include a comprehensive analysis of short-term instability due to noise in electronic oscillators, a new systemic approach to clock synthesis and tuning, a CMOS-compatible RF MEMS process technology, a high-performance clock synthesizer, an IP-based and top-down design methodology for microsystems, and one of the first RF MEMS synthesis tools.

Perhaps, though, the most significant contribution of this work is the approach with which this technology was developed. The primary thrust of this work has not been to optimize one critical metric, such as Q, as is often the case in related research. Rather, this work has been focussed at a systemic approach to achieving monolithic clock generation with high performance. Consequently, the performance of the developed clock synthesis system is outstanding across several metrics. This fact is best captured by direct comparison with state-of-the-art clock synthesis implementations, which are discussed in the following sections.

8.2 Comparison to State-of-the-Art

The monolithic free-running approach and the hybrid crystal and PLL approach to clock synthesis are the two most appropriate implementations for direct comparison to this work, as these two approaches are by far the most common. In the following two sections, measured performance from this work is compared to both recently published research and commercial products.

8.2.1 Comparison to Recent Research

In [140], the performance of a free-running ring VCO is reported. Although the target application for the work in [140] is predominately wireless, the performance reported can be compared directly to the work in this dissertation because this ring VCO could be easily utilized in a clocking application. Using [140] as a benchmark is also useful because the work has been published relatively recently and thus provides an indication of the current performance achievable with a ring oscillator. Similarly, a very recent CMOS PLL clock synthesizer has been reported in [141]. This implementation does not actually interface directly to a crystal reference, but rather to an off-chip clock. Thus the output signal in [141] is phase locked to this reference signal. A summary of the performance of both of these implementations as compared to this work is presented in Table 8.1. Some of the most notable observations include the following:

Metric	[140]	[141]	This work
Output frequencies (MHz)	661.5 - 1,270	880 - 1,648	28, 56, 111, 223, 446
Frequency accuracy	NA	Set by ext. clock	$f_o \pm 0.75\%*$
Temp. stability (ppm/°C)	NA	-200	-77
Worst case duty cycle	NA	NA	51/49
Phase noise (dBc/Hz at offset from f_o)	-106 at 600kHz from 900MHz	NA	-105 at 100kHz from 891MHz
Worst case period jitter (ps)	NA	11	2
Worst case period jitter (ppm)	NA	13,750	280
Tuning range	48%	87%	2.2%
Power supply (V)	2.5	3.3	1.8
Bias current, no I/O (mA)	6.2	33	8.8
Power supply sensitivity	298%	6.0%	6.9%
Power, no I/O (mW)	15.4	109	15.8
Norm. power to f_{max}, no I/O (mW/MHz)	0.012	0.066	0.035
Process technology	0.5μm CMOS	0.35μm CMOS	0.18μm CMOS
Die size (mm^2)	0.013	1	1
External components	None	Driven by ext. clock (19.44 and 77.76MHz)	None
PLL	None	On-chip	None
Max. multiplication or division factor	1	×64	÷32

Table 8.1 Comparison of critical metrics between this work and two recently published implementations. [140] is a free-running ring VCO. [141] is a hybrid frequency synthesizer requiring an external clock reference at the frequencies indicated. Frequencies are synthesized on-chip with a PLL and ring VCO. NA = not available. *Frequency accuracy reported here is "out-of-fabrication" with no tuning.

- The area and normalized power for the free-running ring VCO are exceptionally low.

- The area required for a PLL is comparable to the area required for this work. However, the PLL work in [141] was developed in a process generation with a geometry that is twice as large as the process geometry used in this work. Nevertheless, the area of the PLL is likely dominated by components such as resistors and capacitors, which do not scale substantially with process generation.

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- The tuning range for both the free-running and PLL implementations is very wide. However, the power supply sensitivity of the former is unreasonably high.

- Although not reported, the frequency accuracy of the free-running VCO is certainly very poor, as can be seen due to the tremendous sensitivity to power supply variation. Likely temperature sensitivity is also high.

- The short-term stability of this work is superior to both implementations. Jitter is degraded in [140] primarily due to the large multiplication factor. Also, upon investigation of [140], it appears that the trigger jitter was not subtracted from the reported measurement and thus the number here is likely an overestimate.

- The PLL implementation is temperature compensated and yet the uncompensated performance of this work is superior.

- The free-running VCO and the PLL implementations provide a much broader tuning range than this work. However, in this work, a broad range clock frequencies can be synthesized by frequency division as was shown.

The work developed in this dissertation clearly possesses distinct advantages as well as some short-comings when compared to this recently published work. The most notable contrast is with the normalized power dissipation and the size of the ring VCO as compared to this work. However, so many of the other performance metrics for the ring VCO are undesirable for clock generation that this solution is not a good candidate for monolithic free-running clock generation. In fact, a better comparison can be made with the performance of commercial clock products, which is covered next.

8.2.2 Comparison to Commercial Clock Synthesizers

The MOI-2000 is a monolithic and temperature-compensated phase shift clock synthesizer available from *Micro Oscillator Inc.* [38]. This is a free-running oscillator that is capable of generating clock frequencies from 3 to 12MHz. The performance of this part, based on

Metric	MOI-2000 [38]	MK3235 [142]	This work
Output frequencies (MHz)	3, 6, 12	3.686, 14.3	28, 56, 111, 223, 446
Frequency accuracy	$f_o \pm 0.5\%$	Set by XTAL	$f_o \pm 0.75\%$*
Temperature stability	$f_o \pm 0.5\%$ 0-70°C	Set by XTAL	$f_o \pm 0.6\%$ 0-100°C
Worst case duty cycle	40/60	45/55	51/49
Worst case phase noise (dBc/Hz at offset)	NA	NA	-110.5 at 100kHz
Worst case period jitter (ps)	NA	500	2
Worst case period jitter (ppm)	NA	~7000	280
Tuning range	0%	0%	2.2%
Power supply (V)	5	5	1.8
Bias current, no I/O (mA)	1.6	9	8.8
Power supply sensitivity	NA	NA	6.9%
Power, no I/O (mW)	8	45	15.8
Norm. power to f_{max}, no I/O (mW/MHz)	0.67	3.1	0.035
Process technology	NA	NA	0.18μm CMOS
Die size (mm^2)	2.38	NA	1
External components	None	32.768kHz XTAL	None
PLL	None	On-chip	None
Max. multiplication or division factor	÷4	×437	÷32

Table 8.2 Comparison of critical metrics between this work and two commercial clock products with different implementations. The MOI-2000 is a free-running monolithic phase shift oscillator. The MK3235 is a hybrid crystal + PLL clock synthesizer. NA = not available. *Frequency accuracy reported here is "out-of-fabrication" with no tuning.

data published in [38], is listed in Table 8.2. A crystal and PLL approach is also listed in Table 8.2. The MK3235 is a clock synthesizer product available from *Integrated Circuit Systems Inc.* [142]. This part synthesizes clock signals at 3.686MHz and 14.318MHz clock from a 32.768kHz crystal reference. Some of the most notable comparisons include the following:

• The uncompensated temperature stability of this work nearly matches the performance of the temperature-compensated MOI-2000.

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- The multiplication factor used by the PLL in the MK3235 severely degrades the jitter and thus this work has far superior jitter even though the MK3235 utilizes a crystal reference.

- Only this work provides the ability to tune the clock frequency.

- The normalized power dissipation for this work, in units of mW/MHz, is almost 20 times less than either commercial implementation.

The remainder of the available performance metrics are comparable across all three implementations. The exception is for the MK3235 where the frequency accuracy and temperature stability is set by the crystal reference. More than likely, this performance will be far superior to the work developed here.

8.2.3 Discussion

For the research applications discussed in this dissertation, size, weight, and cost restrictions were motivating factors for eliminating the off-chip crystal and on-chip PLL. The comparisons drawn in Table 8.1 and Table 8.2 clearly indicated that this work provides the best clock synthesis performance over the broadest range of metrics, while at the same time eliminating all off-chip components. However, the ring VCO has been shown to provide the lowest power, smallest area, and broadest tuning range. Nevertheless, the power supply sensitivity, and temperature sensitivity make this an unattractive option for clock generation. Most importantly, though, ring VCOs do not provide the frequency accuracy and stability required for clock generation in most applications. For these reasons, this work appears to be one of the best candidates for monolithic clock generation in the future.

8.3 Future Research Topics

Although the prototype development in this work was successful, there are certainly many performance metrics that can be improved. For example, the power supply sensitivity can be reduced greatly and techniques by which this goal can be achieved have already been proposed in this work. Similarly, a temperature compensation approach has already been

described. These enhancements merely require implementation as the theoretical approaches have already been determined.

One particularly interesting topic that warrants further investigation is a comparison of the frequencies synthesized in the top-down approach present in this work to the frequencies synthesized in a PLL, or bottom-up, approach. In a bottom-up approach it is trivial to synthesize clock frequencies that are integer multiples of the base reference frequency. This approach gives rise to output frequencies of the form,

$$f_{out} = N f_{ref} \tag{8.1}$$

where f_{out} is the output frequency, f_{ref} is the reference frequency, and N is an integer. In contrast, the frequencies synthesized in this approach are of the form,

$$f_{out} = \frac{f_o}{2^N} \tag{8.2}$$

where f_o is the oscillator core frequency. Clearly the synthesized frequencies are not of the same form in the two approaches. In many applications, such as in the microsystem developed in this work, this is not significant. However, in other applications, it is desirable to be able to change the clock frequency by the relationship described in (8.1). An alternative system architecture is required for these applications in order to utilize the proposed top-down system. This is not as difficult as it may first appear. In fact, fractional frequency synthesis approaches, such as phase switching [111], allow frequencies of the following form to be synthesized,

$$f_{out} = \frac{M}{N} f_o \tag{8.3}$$

where both M and N and integers. These integers can be selected such that the synthesized frequencies match, or are very close to, those given by (8.1). This approach warrants further exploration.

Another significant topic that warrants further research is minimization of the power dissipation. This is particularly important when considering low-power stand-by
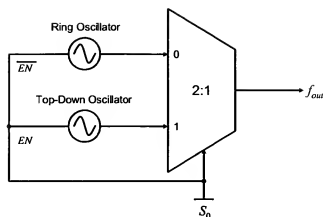
Figure 8.1   Schematic of a low-power clock synthesizer using a ring oscillator for stand-by mode.

operation of a processor. In such a mode, the clock frequency is often reduced to kHz frequencies. Although the developed clock synthesizer has been shown to be able to generate such frequencies, the power dissipation is quite high because the core continues to run at GHz or MHz. An architectural approach can be considered in this case where at some crossover frequency, a ring oscillator is switched on in lieu of the top-down clock synthesizer. The ring oscillator can generate the clock at much lower power, but with poor frequency accuracy and stability. However, while a processor is in a stand-by mode, this is insignificant. Similarly, when the processor clock frequency is returned to full speed, the ring oscillator can be deactivated and the top-down clock synthesizer can be enabled, thus providing high frequency accuracy and stability. A schematic of such an implementation is shown in Figure 8.1.

One final topic that warrants further research is the development of an automatic trimming technique. If this clock synthesizer is utilized in a high volume application, then some fast technique by which the frequency can be trimmed is required. This can likely be accomplished with some relatively simple logic that takes a clock signal from a known off-chip reference and compares it to the monolithic reference. The logic can then automatically adjust the frequency of the monolithic reference using the frequency pulling method described in this dissertation.

8.4 Concluding Remarks

A high-performance monolithic clock synthesis system has been developed successfully in this work. Topics that warrant further investigation were presented in the previous section. It is the authors aim that the synthesis approach developed here be refined to a point where its use becomes commonplace. Such ubiquity is certainly the ultimate test of the utility of any technology.

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